1955

A system for producing a pulse amplitude modulated, time division multiplex signal using semi-conductor devices.

Clarke, Horace Donald

Monterey, California: U.S. Naval Postgraduate School

A SYSTEM FOR PRODUCING
A PULSE AMPLITUDE MODULATED,
TIME DIVISION MULTIPLEX SIGNAL
USING SEMI-CONDUCTOR DEVICES

Horace Donald Clarke, Jr.

UNITED STATES
NAVAL POSTGRADUATE SCHOOL

1909

THESIS

A SYSTEM FOR PRODUCING A PULSE AMPLITUDE MODULATED, TIME DIVISION MULTIPLEX SIGNAL USING SEMI-CONDUCTOR DEVICES

-by-

Lieutenant Horace D. Clarke, Jr., U.S.N.

A SYSTEM FOR PRODUCING A PULSE AMPLITUDE MODULATED, TIME DIVISION MULTIPLEX SIGNAL USING SEMI-CONDUCTOR DEVICES

* * * * * * *

Horace D. Clarke, Jr.

A SYSTEM FOR PRODUCING A PULSE AMPLITUDE MODULATED, TIME DIVISION MULTIPLEX SIGNAL USING SEMI-CONDUCTOR DEVICES

by

Horace Donald Clarke, Jr.
Lieutenant, United States Navy

Submitted in partial fulfillment
of the requirements
for the degree of
MASTER OF SCIENCE
IN
ENGINEERING ELECTRONICS

United States Naval Postgraduate School
Monterey, California

1955

This work is accepted as fulfilling
the thesis requirements for the degree of

MASTER OF SCIENCE

IN

ENGINEERING ELECTRONICS

from the

United States Naval Postgraduate School

Appr

PREFACE

In 1853, Moses B. Farmer patented a system for the transmission of several telegraph messages over a single line, by the allocation of independent intervals of time to the transmission of each message. This was the birth of time division multiplex as we know it today. In 1920, John R. Carson demonstrated the sampling theorem, as it is now known, showing that by sampling a signal at a rate slightly in excess of two times the highest frequency contained, all the information required to reproduce the signal was present. This specified the sampling rate as it is presently used. Various time division multiplex systems were developed during the following years, but with the advent of the transistor, new emphasis was placed on these systems in an effort to construct portable time division multiplex terminals. Application was impractical until 1951 when junction transistors appeared and quantity production with uniform characteristics of this type and the older type of point contact transistor became possible. The transistor features of low power drain, high efficiency, ruggedness, long life and small size made a portable system feasible.

This paper presents a system, different, to the writer's knowledge, from any heretofore used for producing a Pulse Amplitude Modulated, Time Division Multiplex signal. The design considerations and resulting performance of a breadboard model are discussed. Several of the equipment features, and in particular one feature, have shown

enough promise to warrant further investigation towards possible future application to military equipment. The material contained in this thesis is largely based on work performed under a U.S. Army Signal Corps contract #DA36-039-SC-64459, Time Division Multiplex Systems, at the laboratories of the Engineering Products Division, Radio Corporation of America, Camden, New Jersey during January, February and March, 1955.

The writer wishes to acknowledge the guidance and encouragement afforded him during this period by the following members of the Radio Corporation of America, Engineering Staff: Dr. H. J. Woll, Mr. K. E. Palm, Mr. D. E. Deuitch, and Mr. R. E. Hickson.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (CONT.)

LIST OF ILLUSTRATIONS (CONT.)

Photograph

LIST OF ILLUSTRATIONS (CONT.)

TABLE OF SYMBOLS AND ABBREVIATIONS

(Listed in the order of their use in the text)

PAM - Pulse Amplitude Modulation (or Modulated)

PWM - Pulse Width Modulation

PPM - Pulse Position Modulation

RC - Resistance Capacitance

μsec - Microsecond

kcs - Kilocycles per second

I_{co} - Common base connection, zero input collector current

KΩ - Kilohms

db - Decibels

^{o}C - Degree Centigrade

dc - Direct Current

μh - Microhenries

V_e - Emitter potential

I_e - Emitter current

$r_{bo}(r_b)$ - Transistor base resistance in the cutoff state

R_b - External base resistance

r_{eo} - Transistor emitter resistance in the cutoff state, consisting of the emitter material resistance and the back impedance of the emitter-base diode.

E_{ee} - Emitter supply potential

R_e - External emitter resistance

E_s	- Emitter potential in saturation state
E_v	- Most negative emitter potential in the curve from transition to saturation
N curve	- V_e versus I_e curve for a point-contact transistor
E_{bb}	- Base supply potential
V_{off}	- Emitter potential at the cutoff operating point
V_{on}	- Emitter potential at the on-state operating point.
$\alpha_{ce}(\alpha)$	- Low-frequency current gain factor in the common base connection
r_{es}	- Transistor emitter resistance in the saturation state, consisting of the emitter material resistance and the forward impedance of the emitter-base diode.
r_{bs}	- Transistor base resistance in the saturation state $\doteq r_{bo}$
I_c	- Collector Current
r_c	- Transistor collector resistance in the transition state, consisting of the collector material resistance and the back impedance of the collector-base diode.
R_c	- External collector resistance
E_{cc}	- Collector supply potential
I_b	- Base current
I_c	- Collector current
$V_{t\ off}$	- Trigger-off voltage
$V_{t\ on}$	- Trigger-on voltage
$I_{c\ mean}$	- I_c value for no modulation

$\alpha_{cb}(\beta)$ - Low frequency current gain factor in the common emitter connection

R_{in} - Resistor comprising series elements of the "or" gate

r_{cx} - Resistance of collector material (extrinsic to the junction)

r_c - Intrinsic collector-base junction resistance

r_{ex} - Resistance of emitter material (extrinsic to the junction)

r_e - Intrinsic emitter-base junction resistance

μa - Microamperes

R_m - Matrix elements (resistors)

I_{DO} - Common emitter connection, zero input collector current

CHAPTER I

INTRODUCTION

In Time Division Multiplex Systems, PAM plays a large role since it may be the output signal or it may be used as an intermediate step in the generation of PWM or PPM. There are two major functions to perform in producing PAM: generation of channel periods and generation of amplitude modulation during those periods. Before such a system can be designed, the number of channels and the highest frequency to be transmitted must be specified. The system to be described in this paper (Figure 1 shows a functional block diagram) employs: two closed ring counter circuits whose outputs are matrixed together to provide the channel periods, recurring at a sufficient rate to ensure adequate sampling of the voice channels; and 24 single transistor audio gates activated by these channel periods to provide the PAM. The closed ring counters have output periods accurately controlled by a divided down, crystal controlled frequency and are ensured of the presence of only one pulse in the ring at any time. The matrix is a passive device, and, therefore, cannot affect the timing accuracy derived from the crystal oscillator. The gate circuit has a period controlled by the pulse from the matrix, distorts the sampled output by less than one per cent over three-fifths of its period, and exhibits extremely small output when the audio is not present. Detailed attention is not paid to the circuits driving the ring

counters as they are fairly conventional and did not require extensive design effort. The system achieves a reduction in the number of transistors employed by previously designed systems, and a simplicity of circuits; both of these generally increase reliability.

Transistors are well suited for ring counter operation. The ring counter has crystal controlled timing accuracy and will be more accurate than a corresponding delay line circuit with its buffer amplifiers, where all channel widths are controlled by a single pulse. The counter scheme employed is a closed ring system switched by turn-off pulses. A common terminal circuit prohibits more than one transistor being on at a time.

Matrices have commonly been used in computers for the generation of timing signals, resulting in a greater number of outputs than the number of driving units. For example: ten transistors arranged in a ring provide ten outputs, whereas the outputs of four transistors and six transistors matrixed together provide 24 outputs. This greater number of outputs is achieved at a cost in output amplitude. The matrix employed uses all resistances, which must be large to provide isolation between the rings. It is inherently more reliable than a matrix using diodes.

Semiconductor gates are generally composed of diodes and provide excellent isolation at the price of high driving power. The single transistor, symmetrical gate of this paper, has an extremely low insertion loss to the audio signal and is essentially distortionless.

Operation is along the forward and reverse collector voltage saturation line giving good linearity under operation conditions, and extremely small output when no audio is applied. The grounded emitter connection of a junction transistor is employed for low input current requirements, resulting in very low current drain from the matrix and, therefore, from the ring counters.

PROBLEM AND POSSIBLE SOLUTIONS

In time division multiplex, the modulation is generally accomplished in one of the following three ways: PAM, PWM, or PPM. In a time division PAM system there are two main problems: the generation of a timing interval, and the generation of modulation in that interval. The sampling rate is fixed by the highest audio frequency to be used and the channel interval determined from modulation considerations. For the particular application at hand, the highest audio frequency is considered to be 3500 cycles per second. Since at least two samples per cycle must be taken, the sampling rate was chosen as 8.33 kcs. This sampling rate must be fixed. Therefore, the basic oscillator frequency should be very stable. The necessity of synchronizing the local oscillator in the receiver places an additional requirement upon the oscillator frequency stability. The timing accuracy can be derived from a 200 kc crystal oscillator and 24 channels can be taken from this basic frequency after frequency division, resulting in a channel

interval of five μsec occurring once every 120 μsecs. The interval length must be accurately controlled since a wide interval will increase cross modulation in the next channel. During this interval, the output is a pulse. It is required that, in the condition of no modulation, the pulse output for a channel be of a fixed amplitude.

There are two broad ways to generate the timing interval: first by sine wave, and second by pulse. Figure 2 shows a method employing a sine wave. The sine wave travels down a fixed phase shift RC line. There are 24 channel outputs, each channel separated in phase by 15 degrees. There are 12 RC networks in the line, each network having one tap. This tap is an output for the traveling positive half cycle of the sine wave input for 12 positions. The transformer in the output of this tap inverts the signal to give the same polarity output for the remaining 12 channels when the oscillator input is traveling on the negative half cycle. Figure 3 shows a lumped constant LC delay line for producing the 24 channel output. Each channel output is separated 15 degrees in phase from the adjacent channel output. The output at channel number 12 is returned to the input through a transformer and an amplifier, or that at channel number 24 is returned to the input through an amplifier and the arrangement becomes an oscillator. The frequency of the oscillation is set by variable inductance, controlled by d-c current flow through the iron core inductors. Figure 4 shows a pulse application, controlled width 24 stage open ended counter for generation of the timing interval. The 200 kcs oscillator drives a

pulse generator which in turn drives a master flip-flop. The two outputs of this master flip-flop are used as turn off signals on the stages of the step counter. A pulse is started in the step counter in an arrangement which consists of a ÷12 chain driving a gate. The output of this gate enables the first stage of the step counter. This is called a set signal arrangement. The outputs of this counter are used to drive 24 separate gates whose outputs are summed together for the multiplex wave train output. Figure 5 shows a variation of the applications in Figure 4 in that a closed ring counter is used in place of the open ring counter. The counter arrangement must be such that one unit is on at all times to initiate the ring action. Figures 6a and 6b use a matrix to combine the outputs of two ring counters. Arrangement is such that only one unit of each ring can be on at a time. The matrix outputs drive gates whose outputs are summed in the load. The voltage across the load is the multiplexed wave train. As shown in Figure 6a, the four by six matrix requires two drives, one for each closed ring counter. The three by eight matrix, shown in Figure 6b, requires only one drive. This drive is for both the three ring and the eight ring. In either event, the turn off pulse feature utilized in Figure 4 is employed. Either matrix of Figure 6 requires that the pick off circuit, in this case the gate circuit, be able to differentiate between two different voltage levels. This is because the poles of the matrix have present both, one or no ring output signals. Figure 7a shows a one matrix timing interval generator

employing three two-transistor flip-flops which divide by two and one four transistor flip-flop which which divides by three. The outputs of all these flip-flops are matrixed together in one large matrix. The pickoff circuit in this case must be able to differentiate between the levels of five outputs and six outputs. In Figure 7b, the same flip-flops drive three matrices. In each matrix, it is required that the output pickoff circuit be able to distinguish between levels of zero, one and two. Figure 8 shows non-controlled width, timing interval generation. An oscillator drives a pulse generator whose output drives a 24 output delay line, with delay equal to five μsec.

A method of generating pulse amplitude modulation is to use 24 audio gates and one common load. The audio gates each receive the five μsec sequenced intervals and pass audio producing five μsec samples of the audio waves. Each five μsec sample has a repetition rate of once every 120 μsecs.

CHOSEN SOLUTION

The solution chosen, for a system to generate the multiplex wave train, is as follows: an oscillator and pulse generator arrangement drives a flip-flop; the output of this flip-flop drives a six transistor ring counter (Figure 10) and another flip-flop; the output of this second flip-flop drives a four transistor ring counter; these ring counters both feed a four by six matrix (Figure 9); the 24 matrix

outputs control 24 symmetrical series gates (Figure 11); the outputs of these series gates are taken in common to the load where their addition is the multiplexed wave train.

The four by six matrix consists entirely of resistances and gives 24 separate outputs one at each pole of the matrix. Since there are no active or non-linear elements in the matrix, it is inherently reliable. Diodes in a matrix, though commonly used, can fail. The result of using diodes is essentially isolation and this is achieved in this solution by the gating device. The matrix outputs are of levels zero, one and two as opposed to the levels zero through six occurring in the matrix associated with the two, two, two and three divider arrangement. The fact that the entire output at each matrix pole is not useable due to the biasing of the gating device may appear to be a disadvantage. This is not the case, however, since it would be impossible to use the entire collector current of the rings and still retain enough current to drive the next transistor of the ring into conduction. This would not be the case if only voltage levels were required. In transistor work currents must be supplied and this loads the ring collectors. Since it is not desirable to drain much current out of the ring collectors, high matrix resistance values must be employed. This will afford good isolation between collectors, will produce a current output to the load, and a linear addition is obtained in the load equivalent resistance.

In the ring counters, point contact transistors are used requiring

only half the number of transistors as would be required had junction transistors been used. The point contact units are admirably suited to counter application in that they exhibit good high frequency characteristics (fast rise and fall times). The use of the common emitter line and common emitter load eliminates the requirement of a reset signal. In the three by eight ring-matrix combination both rings are driven from the master flip-flop. At first glance this would appear to be a better system, however, the longer ring is less reliable. In the four ring by six ring arrangement, the four ring is driven by the master flip-flop. Increased reliability results from the use of a ring consisting of two less units since the combined back impedance of the off transistors will tend to lower the impedance of the emitter supply source [2]. It is felt that the disadvantage of two drive circuits is relatively unimportant as compared to the increased reliability. There is a saving of one transistor by using the four by six arrangement in preference to the three by eight arrangement. Point contact transistors are generally not as uniform nor as reliable as junction transistors, however, a saving of one transistor in each counter stage results from their use.

The symmetrical series gate employing a symmetrical transistor was chosen in preference to a symmetrical shunt gate or a diode gate. The use of a symmetrical gate results in low loss to the audio signal while passing through the gate. The gate can be reverse - biased to act as an effective diode eliminating the need for isolating diodes between

it and the matrix output. The symmetrical feature has the advantage of giving no output when no audio input is present even though a pulse is applied to the input circuit. The series gate has an inherent advantage over the shunt gate in that it can feed a common load. The shunt gate cannot feed a common load unless an additional "or" gate is inserted in common in the outputs. The isolation afforded to the matrix by reverse biasing the gate results in a load applied to the collectors of the ring counters only at an output level which is above the minimum required to perpetuate the count in the closed ring. The positive pulse matrix output dictates the use of N-P-N transistors in the series gates since only in saturation will the series gate be low loss to the audio signal. An N-P-N transistor exhibits adverse storage effects when coming out of saturation and this results in cross-modulation since the pulse trails off into the next channel. A high frequency P-N-P symmetrical transistor could be employed with a negative pulse matrix output, were one available. The need for a high frequency symmetrical transistor is indicated.

CHAPTER II

DRIVING CIRCUITS

1. Oscillator

The oscillator is a crystal controlled, feedback type, grounded base stage with a grounded collector stage in the feedback path for impedance matching [10] of the grounded base output to its input, as shown in Figure 12. The output of the oscillator is taken across a high impedance tuned load. The input signal is taken from this point and a-c coupled to the high impedance input of the grounded collector stage. The low impedance output of the grounded collector stage feeds the low impedance input of the grounded base stage through a series connected, 200 kcs. crystal. Since the grounded collector circuit provides no voltage gain, its entire purpose is impedance transformation for efficient feeding of the grounded base stage. The grounded base stage supplies the entire output. D-c stabilization, to protect against changes in I_{co} and temperature, is provided in each stage by (1) a 100 KΩ resistor from base to collector supply in the grounded collector stage (2) a ten K Ω resistor to the collector supply and a 2.7 K Ω resistor to ground from the base of the grounded base stage. Direct current bias setting of the grounded base stage is provided by the ten K Ω and one K Ω (from emitter to ground) resistors in the grounded base stage. This results in class C oscillator operation into the tuned load. The circuit is designed for N-P-N

junction transistors operating at collector voltage of +20 volts. Texas Instrument Silicon junction transistors, having very small I_{co} and needing only the simplest form of d-c stabilization, were used. The circuit performed equally well with a random group of silicon types 901, 904, 904A, and 905 transistors.

The crystal frequency was 200 kilocycles. An output load of ten K Ω reduced the output voltage by two db and a two K Ω load was the heaviest that could be used and still obtain satisfactory operation. The open circuit output voltage was 16.5 volts peak-to-peak for a collector supply of 20 volts. The output amplitude was flat to within one db under temperature conditions from $-60^{\circ}C$ to $+70^{\circ}C$. A seven cycle frequency shift was observed over this temperature range. A six cycle frequency shift resulted from changing supply voltages from five volts to 23 volts.

Though the circuit uses two transistors instead of the one normally necessary for an oscillator, it is deemed worthwhile in cases where extreme reliability is required. The feedback path amplifier keeps the output voltage at a high level under varying conditions.

2. Pulse Generator

The pulse generator is an overdriven amplifier followed by a peaking and clipping circuit. A grounded emitter stage (Figure 13) is used to provide current gain at small driving current input without mismatching the oscillator output during the period when the

amplifier is not saturated by the overdriving base signal. The stage is d-c stabilized by a 8.2 KΩ resistor from the base to ground and employs a Texas Instrument 900 series silicon N-P-N transistor at a collector supply potential of +20 volts. The peaking is accomplished by a shunt connected inductance in preference to a series capacitor to provide a wider pulse output. The negative signal from the collector, when the transistor goes on, is passed to the load, while the positive signal resulting from the transistor cutoff is shunted to ground by a diode. The diode is a silicon unit, chosen for its extremely high back resistance and relatively low forward resistance. The output is a series of negative pulses occurring with the positive swing of the oscillator output. The output waveform base line is diode clamped to ground. Sufficient isolation between the oscillator and the following flip-flops is achieved by the pulse generator.

The open circuit output was 6.8 volts peak and the output to an a-c coupled two KΩ load was 4.8 volts peak. The output rise time was 0.2 μsec. and the fall time was 0.35 μsec. Total base line pulse width was 0.6 μsec. The value of the peaking inductance was not critical, the same output occurring for values greater than 1500 μh.

3. Flip-Flops

The four transistor flip-flop (Figure 14) is used in preference to a two transistor flip-flop because of its increased reliability.

Grounded collector stages are used in the cross-coupling network for impedance transformation in the same manner as was the second stage in the oscillator. The presence of the grounded collector stages reduces the collector loading introduced by the cross-coupling capacitors. Low impedance outputs are available at the emitters of these stages but these outputs proved to be insufficient to drive the following circuits and additional grounded collector stages were inserted after the collector outputs of the flip-flop. D-c stabilization of the grounded emitter stages is provided between collector and base by the "emitter follower" action of the grounded collector stages. The cross-coupling capacitors are large enough to provide regeneration without introducing undue loading effects on the collectors of the grounded emitter stages. All transistors are P-N-P high frequency junction transistors. A negative input trigger is applied simultaneously to both bases of the grounded emitter stages and the action is to turn the "off" unit on. This negative trigger on the base of the "on" unit is overcome and exceeded by the positive going signal coupled from the "off" collector as it is going on. Positive triggers could be used for turning the "on" unit off but this would require a larger trigger since the "on" unit is in saturation. Driving out of saturation requires increased amplitude to overcome the saturated effect. Feeding in a current trigger is accomplished by the 3.3 K Ω series resistors in the input lines.

Experimental, high frequency, P-N-P junction transistors are used

to achieve reasonable rise and fall times. The rise time was 0.3 μsec. and the fall time was 0.5 μ sec. The output collector amplitude on the grounded emitter stage was 16.5 volts peak for a collector supply of -20 volts.

4. Emitter Followers (Grounded Collector Stage)

The emitter followers (Figure 15) serve the function of: (a) impedance matching the output of the flip-flop to the low impedance input of the ring and (b) isolating the flip-flops from the ring. They have no voltage gain but provide current gain. The sharp, positive going leading edge of the flip-flop output is obtained by series capacitor peaking with the negative spike blocked by a diode. The series of positive spikes is reproduced in the output of the emitter follower with the same polarity at essentially the same amplitude by a current dependent on the load requirements. The rise time was increased to 0.4 μ sec. by this circuit.

CHAPTER III

DISCUSSION OF CLOSED RING COUNTERS

The action of any point contact, single transistor circuit, whether bistable, monostable or astable, depends upon a region of negative resistance shown in the transistor characteristics, for example, the V_e vs. I_e curve, [6]. This characteristic is shown in Figure 16. Generally the transition from cut-off to negative resistance is sharply defined, whereas that from negative resistance to saturation will be gradual dependent on the transistor parameters and the type of transistor. The slopes of the negative resistance and saturation regions of this curve depend on values of the external base resistance and the collector load resistance [1]. The zero emitter current point of the curve is determined by the voltage resulting from I_{co} flow through r_{bo} and R_b, together with any external base bias supply used.

The equivalent circuit for the cutoff state is shown in Figure 17, [6]. In cutoff, the transistor operating point lies on the curve of r_{eo} at a point set by the value of $-E_{ee}$. The trigger on requirement is E_{ee} minus I_{co} $(R_b + r_{bo})$, Figure 16. When this trigger-on requirement is exceeded, the transistor goes into the regenerative transition region and rapidly moves into saturation. Operation stabilizes at a point determined by the intersection of the load line for R_e drawn from the cutoff operation point. The trigger-off requirement is E_s, as seen in Figure 16. The equivalent circuit for

saturation is shown in Figure 18. Operation in the saturation region is not advantageous in pulse applications due to the storage phenomenon which causes a delay in the trailing edge of the step of collector current (in response to an off-trigger signal) [8]. This effect is much less pronounced in point contact transistors than in junction transistors, but is still objectionable, ranging up to two μ sec. under heavy saturation [6].

There is, however, a way to keep the transistor from becoming saturated by choosing a value of R_e such that the emitter load line will intersect the N curve in the transition region as shown in Figure 20 [2]. With this type of operation, a non-linear emitter load is often employed, as in Figure 19. The "on" trigger requirement now becomes $E_{bb} - I_{co} (R_b + r_{bo}) - V_{off}$ and the off trigger requirement is $-V_{on}$, as shown in Figure 20 [8].

Suppose that it is desired to place a number of these flip-flops in a closed chain to give a sequenced pulse output. This can be readily accomplished with a ring counter arrangement such that one transistor going off turns the next transistor on and the "on" operating condition is transferred around the ring. For accurate timing of the periods of "on" operating condition, a series of turn-off signals may be applied to the inputs of all transistors. If this were accomplished by pulses applied to all inputs of a closed ring, the transistor which receives the "on" signal from the previous off-going transistor would simultaneously receive an "off" signal. This can be

avoided by differentiating the two outputs of a flip-flop and using them as turn-off signals to be applied to alternate inputs of the transistors in the closed ring [9]. Only one transistor is on in the ring at a time. In the ordinary counter scheme, means for having this is provided by a reset signal. This can be avoided by using a common emitter impedance (figure 10), such that the current flow in the "on" transistor causes a reverse bias on the remaining transistors, cutting them off. The emitter line potential remains fixed due to one transistor being on at all times.

When polarizing potentials are applied, action is initiated by the emitter supply voltage which is of such a polarity that it applies forward bias to all transistors. When a unit conducts there is an immediate drop across the common emitter impedance, causing the common emitter line to be reversed biased relative to the bases of all "off" transistors. The action is instantaneous. Due to α_{ce} greater than one, the collector current will exceed the emitter current and, being in the opposite direction, will cause the base of any "on" transistor to go negative. The base of any "off" transistor, on the other hand, will remain at the cutoff operating point. Since there is a small resistance between emitter and base for an "on" transistor ($= r_{es} + r_{bs}$), the potential of the common emitter line will be slightly positive with respect to the base potential of the "on" transistor. Two transistors cannot come on because the external emitter resistance prohibits saturation and limits the flow of I_e

(c) The values of E_{ee} and R_e determine the "on" state operating point on the characteristic drawn for given values of R_b, R_c, and E_{cc} [1].

(d) The values of E_{cc} and R_c will set the amount of output swing available as seen in the collector characteristics for the "on" state operating I_e.

For uniformity of voltage levels throughout the multiplex equipment, $E_{cc} = -20$ volts and $E_{ee} = +20$ volts were chosen. From the collector characteristics, Figure 22, a value of $R_c = 2.2\ K\,\Omega$ gave sufficient output and did not limit the maximum permissible I_e to too small a value. E_{bb} may assume any value required for back biasing the diodes into the "off" state but it should be small enough so as not to require large driving circuit output voltage. $E_{bb} = +$ one volt was chosen. Since operation is to be in the transition region, a point on the collector characteristic must be chosen for the "on" state. Because R_b is common to the input and output circuits, the current flow through it in the "on" state is $I_b = (I_c - I_e)$ and this acts to reduce V_{cc} to $V_{cc} - (I_c - I_e)\,R_b = V_{cc} - I_c\,(\alpha-1)/(\alpha)R_b$. This can be represented on the characteristics by a line for $V_c = I_c\,(\alpha-1)/(\alpha)R_b$. The sum of points on this line and points on the voltage saturation line (the line on the collector characteristics indicating the limiting approach of V_c towards zero potential without reduction of input current) represents the new saturation condition as shown in Figure 22. The operating point is on the $2.2\ K\Omega$ load line

and is in the transition region between the adjusted saturation line and cut-off. The choices of R_e and R_b were then made on a trial basis because there are three factors to consider: The value of R_b will determine the shape of the N curve, with R_c and E_{cc} already chosen; The I_{co} (read from Figure 22 for the E_{cc} and R_c chosen) flow through R_b and r_b will set the "off" operating point of the curve relative to E_{bb}; and the R_e load line must cross this curve at the value of I_e chosen from the collector characteristics for the "on" operating point. $R_e = 18\ K\Omega$ and R_b = one $K\Omega$ were chosen to match the $I_e = 1.2$ ma and $I_{co} = 1.2$ ma. selected on the collector curve. The N curve for the chosen values of $R_c = 2.2\ K\Omega$, R_b = one $K\Omega$, $V_{cc} = -20$ volts were taken for five 2N22 transistors and an average curve constructed for design work, Figure 23. Values picked off the curve are:

$I_{co} = 1.2$ ma, $I_{eon} = 1.2$ ma., $I_{con} = 4.7$ ma.

$V_{b_{off}} = E_{bb} - I_{co} R_b = - 0.2$ volts.

$V_{b_{on}} = E_{bb} + (I_e - I_c) R_b = - 2.5$ volts

$V_{e_{on}}$ and $_{off} = V_{b_{on}} + I_e (r_{e_s} + r_b)$

The data sheet gives $r_{11} = r_{e_s} + r_b = 250\ \Omega$

$V_{e_{on}}$ and $_{off} = - 2.5 + 1.2 (\frac{250}{1000}) = - 2.2$ volts

Figure 21, showing the transistor equivalent circuit for the "on" operating condition in the transition region [1], is used in arriving at the above equations. Since the emitter potential in the "on" and

"off" states is constant, it operates as a load line on the N curve similar to the load line for a perfect non-linear emitter load. As shown in Figure 23, the operating path goes between the cutoff region curve and the R_e load line at $V_e - E_{bb} = -3.2$ volts. The required turn-on trigger is then equal to V peak $- V_e = + 0.8$ volts on the emitter. The turn-off trigger required on the emitter is $V_{t\ off} = V_{e\ on} - V_e$ peak $= + 1.5$ volts. These same potential changes will cause the change in state when they occur, with opposite polarity, on the base.

The emitter follower which drives the turn-off bus is shown in Figure 15. It has an open circuit output of + ten volts peak amplitude. At the peak of the output waveform, the unloaded output circuit is essentially that shown in Figure 25. The available output current is 2.97 ma. The load on the emitter follower is only the "on" transistor since the 68 KΩ resistors and their series diodes set the emitter follower output base line at $V_{b\ on} = - 2.5$ volts. The available turn-on pulse, determined from a ring collector equivalent output circuit, shown in Figure 24, is 2.41 volts peak. The excess trigger voltage furnished is then 1.61 volts peak. The available turn-off pulse, determined from the emitter follower equivalent circuits, shown in Figure 25 for no-load and in Figure 26 for an "on" ring transistor load, is 2.29 volts peak. The excess trigger voltage present is 0.79 volts peak.

RESULTS AND CONCLUSIONS FOR CLOSED RING COUNTERS

Typical four transistor counter and six transistor counter output waveforms are shown in Photograph #1. A table comparing values is as follows:

	Computed Value	Average Observed Value
I_{co}	1.2 ma.	1.8 ma.
$V_{e_{on}}$ and off	-2.2 volts	-2.89 volts
$V_{b_{on}}$	-2.5 volts	-2.7 volts
$V_{b_{off}}$	-0.2 volts	-0.67 volts
$V_{c_{on}}$	-9.0 volts	-8.4 volts
$V_{c_{off}}$	-17.0 volts	-17.05 volts
V_{out} (peak)	+8.0 volts	+8.65 volts
$V_{t_{on}}$ (peak)	-3.44 volts	-3.425 volts
$V_{t_{off}}$ (peak)	+3.49 volts	+5.8 volts

The basic limitation of this circuit, realizing one can build drive circuits which can meet the turn-off trigger requirement, is the variation of I_{co}. In a sample of 25 2N22 transistors, the average I_{co} measured was 1.74 ma. and the extreme values were 2.3 ma. and 1.0 ma. This is a serious limitation on the 2N22 (1698) transistor because I_{co} may vary with age and will vary widely with temperature. Increasing temperature will increase I_{co}, which will, in turn, further increase the temperature leading to a regenerative

action [3]. The limitation, as far as the ring counter is concerned, lies in the fact that the voltage I_{co} (R_b + r_b) determines the "on" trigger requirement at the base of the "off" unit. A larger I_{co} makes it more difficult to trigger "on" since I_{co} R_b is of different polarity than the trigger. If a transistor with high I_{co} is placed in the circuit with a number of roughly equal I_{co} units, it could not be triggered "on" by the available turn-on pulse amplitude. With transistors of roughly equal I_{co} in use, operation can be achieved by varying R_e. Data was taken to show the position of the valley of the N curve for the selected R_b, R_c and E_{cc}. The range of variation of the valley is shown as a dotted rectangle on Figure 23. This sets a limitation on the smallest value of R_e used to keep the transistors out of saturation, avoiding storage which will delay the cutoff time and cause pulses of unequal width in the output. The upper limit on the value of R_e used is set by the turn-on pulse amplitude required, which varies with the value of $I_{c_{on}}$. $I_{c_{on}}$ is determined by $I_{e_{on}}$ which, in turn, is determined by the R_e load line. The amplitude of the output can be increased by increasing R_c, decreasing the value of R_e or increasing the value of V_{ee} to the point where a transistor goes into saturation; since saturation will pose serious limitations on the minimum turn-off amplitude required [8]. In conclusion, the circuit will fail in high temperature operation because of increasing I_{co} and requires the use of transistors whose I_{co} is close to the average value stated in the manufacturer's data. This I_{co}

limitation could be overcome to some extent by using RCA 2N32 transistors and high temperature operation would be possible up to 50°C.

CHAPTER IV

DISCUSSION OF GATE CIRCUIT

The gate circuits are to be 24 in number, one for each matrix output. The gate is to open in response to the matrix signal during its five µsec period. Use of a single transistor as a gate was considered and many possible schemes were developed. Several important considerations apply to the gates in general and they will be mentioned before considering the individual gates.

There are two main types of gates: the series switch device and the shunt switch device. The series switch is one which opens in response to the input signal and lets the audio through to the load. The shunt switch is one which shunts the audio away from the load until the input signal opens the switch and the audio must flow to the load. Aside from various practical reasons, there is nothing which would cause one type to be preferable to the other, assuming that the resistance representing the loss is constant across the non-conducting switch.

Since the enabling pulse is of five µsec duration, and it is desirable to obtain an output of exactly the same duration in view of the cross-talk problem, the transistor used should be high frequency. Further, it is desirable to use a junction transistor in the majority of operations because it requires low current drive and is more reliable at the present time [5] [9]. When a square pulse is

applied to the input of a transistor, the output will exhibit several detrimental effects, depending on the high frequency response of the transistor and the values of components in the external circuitry. One effect is the rounding of one edge of the output pulse due to the shunt capacity of the transistor and wiring to ground. This effect is shown in Figure 27. When a transistor is driven into saturation, it becomes a low impedance device and when driven into cutoff, a high impedance device [4]. In a P-N-P transistor, the positive going output signal is obtained when the transistor is turned on and driven towards saturation. Since the transistor is a low impedance device when saturated, the RC time of charge decay is very small and the edge is essentially square. When a P-N-P transistor is turned off and goes into cutoff, it is a high impedance device and the RC time of charge decay is large giving rise to a rounded trailing edge. In the N-P-N transistor, the same effect occurs. The difference lies in the fact that the poor negative going edge of a P-N-P transistor is, time-wise, at the same location as the good negative going edge of an N-P-N transistor for a given polarity of input pulse. One type of gate will be preferred to the other to reduce cross-modulation since it is undesirable to have the poor edge decaying into the next channel. A second effect is the rounding of the leading edge of the output pulse. This is observed at the same time in N-P-N or P-N-P transistors and is due to the diffusion time lag represented in an equivalent circuit by the charging up of the series capacity associated with the input circuit

P-N junction [5]. The discharge of this capacity in the equivalent circuit is through the junction equivalent resistance and hence depends on the high frequency characteristics of the transistor. A third effect is known as the storage phenomenon [4]. During saturation, the minority carrier density in the base region increases and at the time of the switching signal this density provides a continuing diffusion current flow causing the switching of the output waveform to lag that of the input. The storage time is influenced by any factor which effects the recombination rate of the minority carriers in the base region.

The gate output must be dependent only on the audio level and not on the size of the input pulse. This is necessary since the output of the gate is PAM and the size of the neighboring pulse on any matrix pole will be a function of the two particular ring transistors feeding it. This requires that the enabling pulse fed to the gate be of less amplitude than that available from any matrix pole for a specified audio input. Then, the enabling pulse must drive the transistor into voltage saturation since, in this way, the collector impedance is low. Means for combating the effect of saturation on the output waveform are required [4]. Shown in Figures 31 and 32 are two equivalent methods using reverse bias. The action here is to increase minority carrier recombination during storage, reducing both the storage time and the storage decay rate. Figure 33 shows a small emitter resistance employed to produce a reverse bias condition during storage and

accomplish the result of Figures 31 and 32 in the same fashion. Figure 34 uses an input capacitor to differentiate both the leading and trailing edges of the input pulse. The trailing edge peak is such as to reverse bias the input junction and decrease the storage time by increasing recombination.

The last major consideration is that of having sufficient enabling pulse current fed into the gate from the ring source available. This problem becomes twofold in that it dictates a required current input setting the value of the matrix resistances. The matrix resistances must not overload the ring collectors, stopping ring count, and must not permit interaction between the ring collectors, giving faulty ring count. Then the saturating, gate circuit input current should be small so that the matrix resistances can be large.

There are two types of gate circuits applicable here, dependent on the manner of variation of the output current and not upon the type of switch, whether series or shunt. Both types depend on operation along the saturation line, as will be explained. These two types are the symmetrical and the non-symmetrical gates, employing a junction transistor.

Basicly, there are two kinds of junction transistors: the grown junction transistor and the alloy junction transistor. The grown junction may be pictured as having a sort of sandwich type construction with emitter and collector junctions having equal areas. Three major differences distinguish the emitter junction from the collector junction:

(1) The gain in the forward direction (nominal connection) is greater than that in the reverse direction; (2) The emitter junction shows Zenner breakdown at much lower potential differences (photograph #2); and (3) The emission efficiency (for the most part dependent on the ratio of hole densities in the two regions) is larger for the emitter junction [7].

The alloy junction transistor has a collector junction area several times larger than the emitter junction area. Holes from the emitter have a larger target area to hit than holes emitted by the collector. In the order of 99% of the holes emitted by the emitter cross the base region to the collector junction whereas the percentage is reduced in the opposite direction [7].

In the non-symmetrical gate, the basic requirement that the output PAM be dependent only on the amplitude of the audio input and not at all on the input enabling pulse, requires that a linear relationship exist between the audio and the output current. On a curve of I_c vs. V_c, this is represented by a line through the origin of coordinates. On the output characteristics of a transistor there is only one line which approximates this condition. Thus, operation must be entirely along the voltage saturation line as shown in Figure 28. The amount of base current required is that corresponding to saturation for the largest audio swing. During the five μsec interval, the audio may have peak amplitude at any time. Therefore, the current input must be a five μsec. pulse of this I_b max. value. The output current variation

for the audio input will be as shown in Figure 28. This current flows through the load indicated by the load line. The circuit requires that the transistor be biased in the usual manner and then there will be a pulse output, indicated by $I_{c\ mean}$, with no audio input. This points up the major drawback for this type of operation--the amplitude of $I_{c\ mean}$ is a function of the saturation resistance (slope of the voltage saturation line) of the particular transistor used in the circuit. This variation would shift the output amplitude of any specified audio input and then, to have a fixed level output for zero modulation, some sort of gain control would have to be employed. This requires 24 controls to set when changing transistors and, in addition, considering that the α_{cb} of the transistor changes with age, temperature etc., the required continuous adjustment makes the scheme unusable.

In the symmetrical transistor, the emitter and the collector are identical and hence can interchange functions readily /‾11_7. When base input is used, the base current will flow in the base-emitter circuit. Since emitter and collector can interchange functions, the base current path can change depending on the potentials of the collector and the emitter. The load and polarizing potential in any base input circuit can be anywhere in the collector-emitter circuit and the transistor will operate. Shifting the polarizing potential from the collector to the emitter does require additional adjustment of the base-emitter circuit for proper bias but this is secondary to present considerations. The operation of a symmetrical gate is depicted in

Figure 29 and the considerations for $I_{b\ max.}$ are as stated in the discussion of the non-symmetrical gate. Now $I_{c\ mean}$ is zero and no output control is necessary to produce a PAM output which is a linear function of the input audio signal when $I_{b\ max.}$ is large enough to produce saturation for the greatest audio swing used.

When an enabling pulse is fed into the gate, its action on the characteristics is to move the operating point from its cutoff position (determined by the audio voltage level), up the load line and on to the voltage saturation line. With changing audio polarity, the transistor changes from the grounded emitter configuration, for a positive polarity, to the grounded collector configuration, for a negative polarity. There is a period at beginning of each pulse when the gate transistor is not in the voltage saturation state but is, instead, in its normal operating state. The output response to a pulse input will exhibit: delay in coming on, rise time decay, storage time, and fall time decay.

Since the output impedance for the common collector configuration is considerably lower than that for the common emitter configuration, the rise and fall times will be considerably less for the negative portion of the output [10]. This effect will not be as noticeable at low audio levels as it is at high ones. The input impedance of the common collector configuration, on the other hand, is considerably higher than that of the common emitter configuration [10]. This will result in less base current input to the common collector polarity

for a given voltage level at the matrix pole. If the voltage available at the matrix pole were a true pulse, the base current would instantly be at its peak value and the transistor would be in the voltage saturated state for any level and polarity of audio not requiring more than this current input. The voltage available, however, exhibits a rise time decay at the start of its five μsec period. This will cause a great reduction in the base current input until the necessary voltage level is reached to supply the base current for voltage saturation. When the matrix pole output has reached a constant level, a.c. conditions will no longer apply and the input impedance of the gate will become so small that it has essentially no effect in determining the current input for either polarity audio. The rise time associated with the output circuit of the gate will then become effective if the transistor is not yet in voltage saturation.

The result of the high gate a.c. impedance will be a reduction in the useful output period corresponding to a delay in the gating action. The delay period will be the sum of the rise time of the matrix pole voltage and the diffusion time lag of the gating transistor. These adverse effects will be extremely noticeable at high audio levels and essentially non-existent at low audio levels.

With operation along the saturation line, symmetry is required only insofar as equal base current inputs for the two connections permit equal collector voltage swings. Poorly balanced transistors could be used in the gate, although inefficiently. The occurrance of the

Zenner breakdown at lower voltage in the reverse connection is unimportant in this application, due to operation entirely along the voltage saturation line.

With these considerations in mind, the symmetrical type gate was chosen. The use of one load posses an additional problem. The outputs of the 24 gates must all feed one input which is a way of saying that there must be one load common to all 24 gates. This requirement immediately eliminates the use of a shunt type gate with common load because there would be one gate on at all times and this would approximate a short circuit continually across the load. An isolation type circuit commonly known as a "or" gate could be used between the gates and the modulator but again this is a transistor amplifier whose output (which is PAM) would be a function of the gain of the particular transistor used. Actually the input circuit of the "or" gate is the essence of what is required and it could be used alone before a load such as a transmitter input circuit. The scheme would be as shown in Figure 30. The drawback to this is that proper isolation is required to hold down crosstalk and large values of R_{in} are indicated. These will attenuate the PAM input to the load.

DESIGN OF GATE CIRCUIT

The open circuit output of each ring collector is, on the average, eight volts. These voltages are added, through series matrix

resistances, in a lower resistance load. Allowing 4.5 volts per collector (3.5 volts required) for the turn-on function in the ring leaves available 3.5 volts at each collector. The current resulting will flow through two paths: the 2.2 K collector load to a.c. ground, and through the matrix resistance and the gate input circuit to ground.

Measurements taken on symmetrical transistors gave the following results: $r_b = 85$ ohms average and $(r_c + r_{cx} + r_e + r_{ex})_{saturated} =$ 29 ohms average, Figure 35 [4]. The subscript "x" stands for the extrinsic resistance; that portion which is not directly connected with transistor action (junction resistance) but is, instead, representative of emitter and collector resistivities. When in saturation, r_c is very low, being on the order of one ohm [4]. Then chosen values for the design are: $r_{ex} = r_{cx} = 5$ ohms, $r_c = 1$ ohm, $r_e = 18$ ohms, and $r_b = 85$ ohms. These are at least correct in the sum and are correct in relative order of magnitude. The exact values are functions of the particular transistor and the particular operating conditions. Their functions in the calculations permit some approximations to be made.

For the circuit of Figure 36, the equivalent input circuit for positive polarity audio at the collector (common emitter configuration) is shown in Figure 37 and that for negative polarity audio at the collector (common collector configuration) in Figure 38. The input impedance is of importance here only insofar as it indicates the matrix loading and the current flow into the base of the gate transistor.

noting the d.c. level at the base for the two conditions, matrix driven and open lead to the matrix. With the d.c. level difference of 0.4 volt at the top of the 68 KΩ resistor and the duty factor of 24, the input current was 141 μ a, pulse. With this base current input, the following figures were obtained on the idealized characteristic, Figure 5: maximum possible audio voltage across the transformer secondary (156Ω equivalent load) for saturated operation was 4.17 volts peak, collector current was 4.0 ma peak, and output voltage was 4.0 volts peak. The base current measured by the base input waveform voltage (photograph #4) across the input circuit was 120 μa using average value parameters in the calculations. This difference in base current indicates that the assumed average values of base and emitter transistor resistances were slightly in error when compared to the values for a particular transistor. Under these conditions, for linear modulation in the positive and negative directions, the audio swing used was 2.2 volts peak. This gave an output voltage swing of 3.7 volts peak to peak corresponding to a collector current of 1.85 ma peak. The following time measurements were made (photograph #5):

Rise time (positive)	1.4 μsec.
Rise time (negative)	0.9 μsec.
Fall time (positive)	1.6 μsec.
Fall time (negative)	0.6 μsec.
Storage time	0.2 μsec.
Starting delay (positive)	0.6 μsec.

impedance gate circuit input for about one µsec. At one µsec., with $\alpha_{cb} = 25$, $R_m = 10\ K\Omega$ and I_{in} max = 100 µa.: I_{in} (common collector polarity) = 16.05 µa. and I_{in} (common emitter polarity) = 66.2 µa. At this time, the positive polarity output should be in its rise time period and the negative polarity output should have started rising for low level audio and still be in the delay time for high level audio.

A Hewlett Packard model 200-C or 202-D audio oscillator, used to simulate the audio input, can supply a swing of 5.5 volts peak across a 200 Ω resistor shunting the secondary terminals of a 1 to 1 transformer. Use of a load resistance of 1 KΩ gives a 6 volt peak to peak gate output (photograph #3) at base current input of 100 µa and audio input of 2.93 volts peak. Use of a common load resistance with one end tied to ground placed the bias arrangement on the input circuit.

Figure 39 is an ideal version of the average collector forward and reverse characteristics showing the $.03^V$ collector to emitter potential difference needed to initiate collector current flow (photograph #5). It shows that saturation over the entire swing will result from a base current input greater than or equal to 100 µa. Using Figure 39, the distortion, in the center two µsec of a five µsec channel, due to (1) the break in the saturation line (photograph #3) and (2) the I_{DO} flow was computed by a five point analysis of the output wave for audio voltage swing of 1.167^V. The third harmonic distortion (which, by this analysis, is the total distortion) was one percent. Figure 40 represents the input and output waveforms used for

impedance gate circuit input for about one μsec. At one μsec., with $a_{cb} = 25$, $R_m = 10\ K\Omega$ and I_{in} max = 100 μa.: I_{in} (common collector polarity) = 16.05 μa. and I_{in} (common emitter polarity) = 66.2 μa. At this time, the positive polarity output should be in its rise time period and the negative polarity output should have started rising for low level audio and still be in the delay time for high level audio.

A Hewlett Packard model 200-C or 202-D audio oscillator, used to simulate the audio input, can supply a swing of 5.5 volts peak across a 200 Ω resistor shunting the secondary terminals of a 1 to 1 transformer. Use of a load resistance of 1 KΩ gives a 6 volt peak to peak gate output (photograph #3) at base current input of 100 μa and audio input of 2.93 volts peak. Use of a common load resistance with one end tied to ground placed the bias arrangement on the input circuit.

Figure 39 is an ideal version of the average collector forward and reverse characteristics showing the $.03^V$ collector to emitter potential difference needed to initiate collector current flow (photograph #5). It shows that saturation over the entire swing will result from a base current input greater than or equal to 100 μa. Using Figure 39, the distortion, in the center two μsec of a five μsec channel, due to (1) the break in the saturation line (photograph #3) and (2) the I_{DO} flow was computed by a five point analysis of the output wave for audio voltage swing of 1.167^V. The third harmonic distortion (which, by this analysis, is the total distortion) was one percent. Figure 40 represents the input and output waveforms used for

the five point analysis.

Cross modulation distortion will result from the I_{DO} flow of the remaining 23 gates through the common load. Since all the "off" gates are heavily reverse biased, the flow in each gate will approach I_{co} and will be of a polarity determined by the audio voltage. The average unit I_{co} is one μa for six volts collector voltage and the worst condition would be 23 μa in the one KΩ load. This d.c. level in the output waveform gave a total even harmonic distortion of 3.05% (by the five point analysis with the drive conditions used to compute the distortion due to non-linear voltage saturation line for 1.165^v peak audio input). Under these circumstances, the total distortion is 3.21%. The distortion due to I_{co} flow can be greatly reduced by increasing the audio drive and at the same time increasing the base current input to the gate. The figure of 3.21% represents the worst anticipated operating conditions during the center two μsec of the channel.

RESULTS AND CONCLUSIONS FOR GATE CIRCUIT

The results for a single gate were obtained in the following fashion: the transistor used has a reverse connection gain equal to 95% of its forward connection gain; a separate source was used to bias the gate, providing accurate control of the saturation current; and the gate was matrix driven. Base current input was measured by

noting the d.c. level at the base for the two conditions, matrix driven and open lead to the matrix. With the d.c. level difference of 0.4 volt at the top of the 68 KΩ resistor and the duty factor of 24, the input current was 141 μ a, pulse. With this base current input, the following figures were obtained on the idealized characteristic, Figure 5: maximum possible audio voltage across the transformer secondary (156Ω equivalent load) for saturated operation was 4.17 volts peak, collector current was 4.0 ma peak, and output voltage was 4.0 volts peak. The base current measured by the base input waveform voltage (photograph #4) across the input circuit was 120 μa using average value parameters in the calculations. This difference in base current indicates that the assumed average values of base and emitter transistor resistances were slightly in error when compared to the values for a particular transistor. Under these conditions, for linear modulation in the positive and negative directions, the audio swing used was 2.2 volts peak. This gave an output voltage swing of 3.7 volts peak to peak corresponding to a collector current of 1.85 ma peak. The following time measurements were made (photograph #5):

Rise time (positive)	1.4 μsec.
Rise time (negative)	0.9 μsec.
Fall time (positive)	1.6 μsec.
Fall time (negative)	0.6 μsec.
Storage time	0.2 μsec.
Starting delay (positive)	0.6 μsec.

Starting delay (negative) 1 µsec.

Since, the entire top of the ideal audio pulse level will probably not be utilized in the load, it was arbitrarily decided to use only one µsec on either side of channel center. The useful portion of the pulse output is then from 1.5 µsec to 3.5 µsec. The distortion in a channel introduced by modulation of the previous channel is due to the positive portion of the decay including the storage time. The decay was completed by 1.8 µsec leaving 0.3 µsec distortion time. The distortion in voltage level at the beginning of this 0.3 µsec period was 1.52%. The rise time portions of a channel introduce further distortion. The positive rise was completed by 2.0 µsec resulting in a voltage level distortion of 4.29% at the beginning of the 1.5 µsec useful interval. The negative rise was completed by 1.9 µsec giving a distortion of 6.32% at the same point due to its longer delay time, even though the decay was faster. There is no distortion at the end of a channel since the transistor is saturated up to and beyond the cutoff point.

Measurements taken on channels 10, 11, and 12, which are time wise adjacent to each other, indicated no voltage level distortion resulting from storage and decay in the previous channel. This is due to the fact that whether a channel is being modulated or not, the base current pulse is still present and makes the collector circuit of that channel a low impedance path to ground shunting the one K Ω load resistor. This shunting impedance consists of the transformer secondary impedance to

a five µsec pulse in series with the "on" gate collector circuit impedance. The total impedance is 40 Ω and the result of its shunting is to show only 3.84% of what would be seen in an open time interval following the gate period. The shunting did not affect the storage time but cut the decay time to 0.5 µ sec. When the matrix feeds several channels with one biasing potential source, the base current input is seriously reduced. This is because the outputs of each matrix pole are not identical in amplitude. The bias must be set at a value which will pass the wanted five µsec interval for the least output amplitude pole and not be so small that it passes some unwanted intervals at high output amplitude poles or the spikes atop these outputs. For five channels, this reduced the usable base current to 70 µa.

CHAPTER V

DISCUSSION OF MATRIX DISTRIBUTOR

A method for obtaining 24 consecutive outputs, which recycle upon completion of each cycle, is to matrix the outputs of two ring counters [2]. The rings may take on different forms in the number of elements of length, provided the product of the number of outputs of one ring and the number of outputs of the other is 24. Specifically, the following arrangements can be used: (1) one by 24, with one drive rate; (2) two by 12, with three possible means of operation (a) the 12 ring driven four times as fast as the two ring, (b) the 12 ring driven two times as fast as the two ring, or (c) the two ring driven two times as fast as the 12 ring; (3) three by eight, with both rings driven at the same rate; and (4) four by six, with the six ring driven two times as fast as the four ring. Demonstration of the firing order and the recycling follows the same principles for each arrangement. For demonstration purposes, only the calculations for the four by six arrangement are included.

To arrive at the firing order of the matrix poles in the four by six arrangement, assume a unit amplitude ring collector output. With time in µsec., the outputs of the collectors of the six ring are:

$\#\,1 \quad \left[u(t) - u(t-5)\right] + \left[u(t-30) - u(t-35)\right] + \left[u(t-60) - u(t-65)\right] + \; +$

$\#\,2 \quad \left[u(t-5) - u(t-10)\right] + \left[u(t-35) - u(t-40)\right] + \; + \; + \; ++$

$\#\,3 \quad u(t-10) - u(t-15) + \; + \; + \; ++$

$\#\,4 \quad u(t-15) - u(t-20) + \; + \; + \; ++$

$\# 5 \quad u(t-20) - u(t-25) + + + ++$

$\# 6 \quad u(t-25) - u(t-30) + + + ++$

The outputs of the collectors of the four ring are:

$\# 1 \quad \left[u(t) - u(t-10)\right] + \left[u(t-40) - u(t-50)\right] + + + ++$

$\# 2 \quad u(t-10) - u(t-20) + + + ++$

$\# 3 \quad u(t-20) - u(t-30) + + + ++$

$\# 4 \quad u(t-30) - u(t-40) + + + ++$

Matrix algebra shows that:

$$\begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \times \begin{bmatrix} 1' & 2' & 3' & 4' & 5' & 6' \end{bmatrix} = \begin{bmatrix} 11' & 12' & 13' & 14' & 15' & 16' \\ 21' & 22' & 23' & 24' & 25' & 26' \\ 31' & 32' & 33' & 34' & 35' & 36' \\ 41' & 42' & 43' & 44' & 45' & 46' \end{bmatrix}$$

For example:

$$\begin{aligned} 11' &= \left[u(t) - u(t-10)\right] \left[u(t) - u(t-5)\right] \\ &= u^2(t) - u(t)u(t-5) - u(t-10)u(t) + u(t-5)u(t-10) \\ &= 1 \quad \text{for } 0 \leq t \leq 5 \text{ since -} \end{aligned}$$

$u^2(t) = u(t) \equiv 0$ before $t = 0$, 1 after $t = 0$

$u(t)u(t-5) \equiv 0$ before $t = 5$, 1 after $t = 5$

$u(t)u(t-10) \equiv 0$ before $t = 10$, 1 after $t = 10$

$u(t-5)u(t-10) \equiv 0$ before $t = 10$, 1 after $t = 10$

Another example:

$$26' = \left\{\left[u(t-10) - u(t-20)\right] + \left[u(t-50) - u(t-60)\right]\right\}$$

times

$$\left\{\left[u(t-25) - u(t-30)\right] + \left[u(t-55) - u(t-60)\right]\right\}$$

$$= 1 \quad \text{for } 55 \leq t \leq 60$$

The firing order before complete recycling is:

	1'	2'	3'	4'	5'	6'
1	1	2	9	10	17	18
2	19	20	3	4	11	12
3	13	14	21	22	5	6
4	7	8	15	16	23	24

The output of any particular pole is one during a five μsec. period, occurring once every 120 μsec. The frequency of a pole output is 1/120 times $10^6 = 8.33$ kcs., which is the sampling rate.

The elements within the matrix are connected to the matrix poles. These elements may be resistors and/or diodes, since isolation between the various inputs is required to ensure proper input circuit operation. One scheme is a diode from each input to each pole with the equivalent load resistance, which might be at a different d.c. level, possibly isolated by another diode. Another scheme is a resistor from each input to each pole and the equivalent load resistance probably isolated by a diode, as before. The scheme selected does not require any diodes and this one fact led to the choice. The avoidance of diodes here is afforded by the fact that the gate acts as a diode, when viewed from the matrix pole. The scheme is shown in Figure 9.

DESIGN OF MATRIX DISTRIBUTOR

The output loads the matrix pole by approximately 20 K Ω when the gate is off and by 107 Ω when the gate is on. From the a.c. equivalent circuits, the heaviest loading is imposed on a ring counter collector when it is driving its own gate "on". With R_m = Five K Ω, the load on a six ring collector is 558 Ω when its gate is "on" and the load on a four ring collector is 750 Ω when its gate is "on". The two ring collectors driving an "on" gate will supply equal voltages to the load at different currents, due to the different loading imposed on each. Reliably, seven volts can be taken, 3.5 volts from each collector, to drive the matrix and gate, leaving enough collector voltage swing to perpetuate ring count. This supplies 176 μ a. gate base current from the six ring and 237 μ a. gate base current from the four ring. The total available base current is 413 μ a.

With R_m = 6.8 K Ω, the six ring collector load is 558 Ω and the available base current is 130 μ a. At the same time, the four ring collector load in 895 Ω and the available base current is 208 μ a. The total available base current for this value of R_m is 338 μ a.

The variation of input current with value of matrix resistance, R_m, is linear in the region of reasonable current inputs because the equivalent loads do not change and there are no additional considerations to change the assumed available collector voltage.

Figure 41 shows the variation and is used to select the value of matrix resistance from considerations of maximum required base current. A value of 9.1 KΩ for R_m giving an available base current of 260 μ a. on this curve will meet the base current requirements and serve as sufficient isolation between ring collectors.

RESULTS AND CONCLUSIONS FOR MATRIX DISTRIBUTOR

At a matrix pole, the outputs of the four ring and six ring collectors were observed to be seven volts peak as compared to the designed eight volts peak. The sum of the outputs at the unloaded matrix pole was 12.5 volts peak instead of the computed 16 volts peak. This limited the useful output to 5.5 volts peak. The design was for a useful output of seven volts peak, corresponding to 3.5 volts per collector. Photograph #6 shows a typical output at an unloaded matrix pole. When the gate circuit was placed as a load on the matrix pole, the output peak was reduced as far as the seven volt level by varying the gate bias level. When several gates were operated from the poles, the peak level moved up in accordance with bias consideration for the gates. Photograph #7 shows a typical matrix pole output driving a gate when five gates were loaded on the matrix. It shows that by no means all of the available 5.5 volt level was utilized.

Both photographs #6 and #7 show the presence of spikes in the

matrix pole outputs. These spikes are in no way connected with the operation of the matrix, but instead are due to input turn-off pulse feed-through in the collector circuits of the ring drivers. The presence of these spikes reduced the useful output to 2.5 volts peak at a pole. This was because the spikes could actuate a gate and amplitude modulation would be observed in the gate output. On a computational basis, with the useful 2.5 volts level, the possible current feed into the base of the gate circuit was 78.5 μa. The actual current feed was observed to be 70 μ a. under conditions of no modulation by the spikes. This low current feed reduced the output possibilities of the gate circuits but this was necessary to avoid the spike feedthrough. Part of the spike feedthrough is due to the action of the ring counter and part is due to the poor grounds in the system. The model from which the waveforms were taken was only a breadboard model and not a finished product, accounting in part for the poor grounding problem, though large bypass capacitors were inserted to help this situation.

The interaction of the waveform on one ring collector, due to a pulse on another ring collector, is negligible. When both collectors feeding a matrix pole are "on" together or "off" together, there should be no interaction because they are at the same voltage level. No interaction was observed. When one collector is "on" and another collector is "off", some interaction should be present, whether the gate is loading the circuit or not. The effect of the six ring

variation on the four ring collector waveform was to produce a small step of amplitude about 2.5% of the four ring collector waveform amplitude. The effect of the four ring collector changes on the six ring collector waveform was negligible.

The matrix provides excellent isolation between the driving rings. Were it not for the presence of the unwanted spikes in the collector waveform, sufficient base current would be available to drive the gates to a large audio output by utilizing more of the matrix pole voltage level. When one gate is fed and there are no other gates in the circuit, and, furthermore, when the action of the spikes is ignored, sufficient output is obtained from the matrix pole to drive the gate well up on the voltage saturation line.

CHAPTER VI

SYSTEM RESULTS AND CONCLUSIONS

In the majority of PAM systems produced in the past, the output, though exhibiting accurate level control relative to the no-modulation level, is a function of the gain of the gating device. This system has its no-modulation output level at ground potential. The output levels for positive and negative inputs are solely a function of the value of the resistance represented by the slope of the voltage saturation line for the gating transistor and the 0.03 volt starting potential associated with germanium transistors. The PAM wave is practically an exact reproduction of the sampled audio input. If it is desired to have the modulated pulses of the same polarity at any specified zero modulation level, as is the case when PAM is converted to PWM or PPM, a fixed d.c. level may be added to the output.

The parameters of the gating transistor are not critical. The gain (α_{cb}) is of small importance as long as the transistor can be operated in the voltage saturation state by the available enabling pulse. The symmetry is a function of the gains of the two configurations used and during the constant output portion of the gating interval a high percentage of symmetry is desirable. The distortion introduced by the gate during the "constant output" portion of its interval is very small and has essential dependence on the 0.03 volt energizing requirement. The gate transistor will exhibit smaller rise

and fall times when a higher frequency transistor is used. Silicon transistors, though available having good high frequency characteristics, do not exhibit any acceptable degree of symmetry (photograph #8). The possible use of low load resistance with small output level change or high load resistance with large output level change gives versatility of load requirements.

A good gating transistor might be defined in this way: α_{cb}, forward connection, ≥ 40; α_{cb}, reverse connection, ≥ 25; degree of symmetry $\geq 62.5\%$; frequency cutoff = 6 mcs.; and the transistor, an N-P-N, grown junction type.

The ring counters would better perform their function of supplying the enabling pulse if high frequency junction transistors were used. A transistor such as that used in the flip-flops would have an essentially square leading edge corner when driven into saturation. The operation of these units in saturation would not place undue requirements on the amplitude of the turn-off pulse since junction transistors require less base current input for switching operation than point contact transistors. The square leading edge corner would, to a large extent, eliminate the starting delay of the gating circuit. The spikes, present in the ring counter outputs, would not be there were junction transistors used. Use of junction transistors would require twice as many transistors as use of point contacts, but the junction transistors have low I_{co} compared to the point contacts and this would considerably enhance turn-on reliability. Higher temperature operation would be possible by

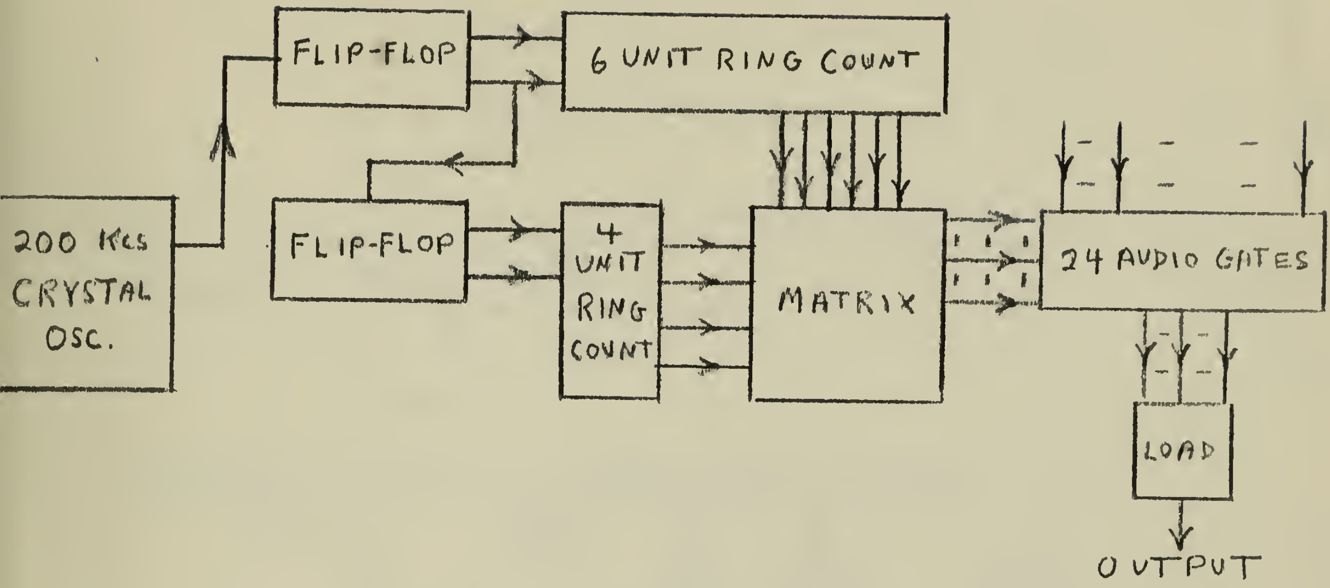
using junction transistors.

The resistors used in the matrix are larger than necessary for isolation purposes. Use of smaller resistors would provide additional output current reducing the symmetry requirements for the gating transistors. The value of the matrix resistors has a linear variation with the output current because these resistors are normally much greater than the input impedance of the gate circuit during the constant output portion of the gate interval.

Photograph #9 shows the output waveform for five channels of the total 24 being modulated. Channels 12 and 18 show the poor trailing edge decay into the following time interval which is not "gated". The second half of this photograph shows the improvement in channel decay afforded by having all 24 channels "gated". Here channels 11 and 17 decay into "unmodulated gated" channels 12 and 18 resulting in superior cutoff of the modulated channels. No modulation is used in order that the effects of channels 12 and 18 on the decay rate may be observed. The useful period of modulation, occurring between two μsec and five μsec, is limited in the beginning by delay and rise time effects. The channel decay into an "ungated" interval uses 1.8 μsec of that interval due to storage and fall time effects, whereas the decay into a "gated" interval uses only 0.4 μsec of that interval due to the same effects. The storage time is essentially uneffected by the presence of a following "gated" interval, as is expected, since nothing has occurred to change the recombination rate of minority carriers.

The decay time has been greatly reduced, however, due to the shunting effect of the following "gated" interval collector circuit impedance. The timing accuracy of the system shows an average starting delay of 0.5 µsec referred to the initiation of rise in the matrix pole output. The matrix output is accurately controlled by the turnoff pulses which derive their basic timing accuracy from the crystal controlled oscillator. The average insertion loss to the audio input is 3.3% for the five gates output. This is less than the computed average loss of 14.3%.

In conclusion, it is felt that this system is a highly competetive one in the field of PAM. The use of junction transistor ring counters, though at least doubling the number of ring transistors used, will vastly improve performance and permit high temperature operation. In the past, high temperature has been the stumbling block for all military transistor applications.



FUNCTIONAL P.A.M. SYSTEM

FIGURE 1

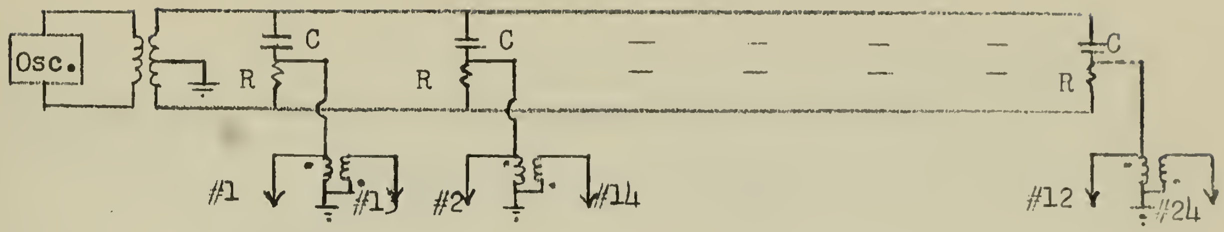


Figure 2

Figure 3

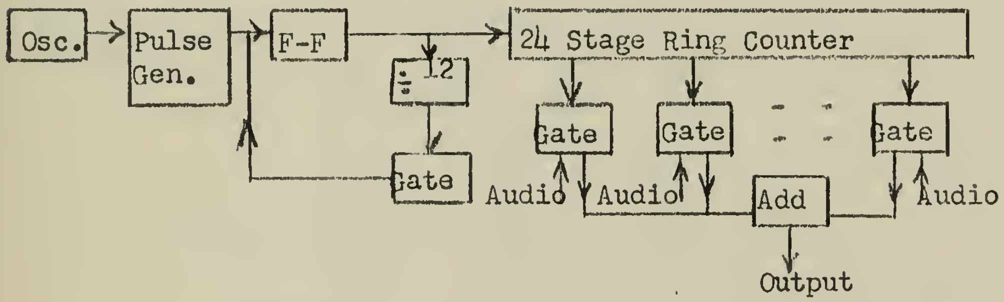


Figure 4

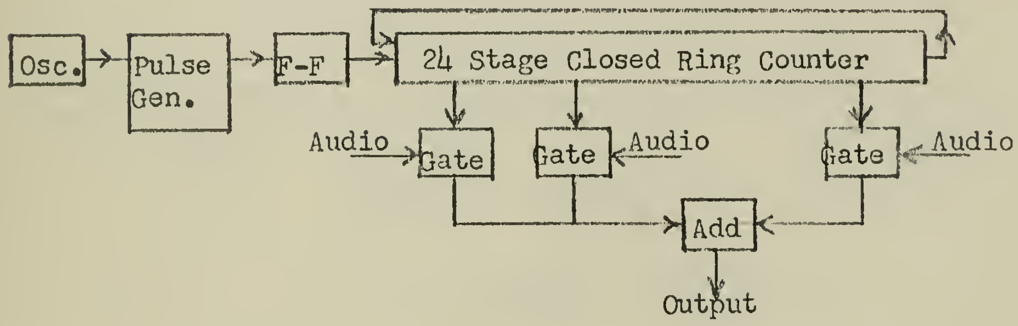


Figure 5

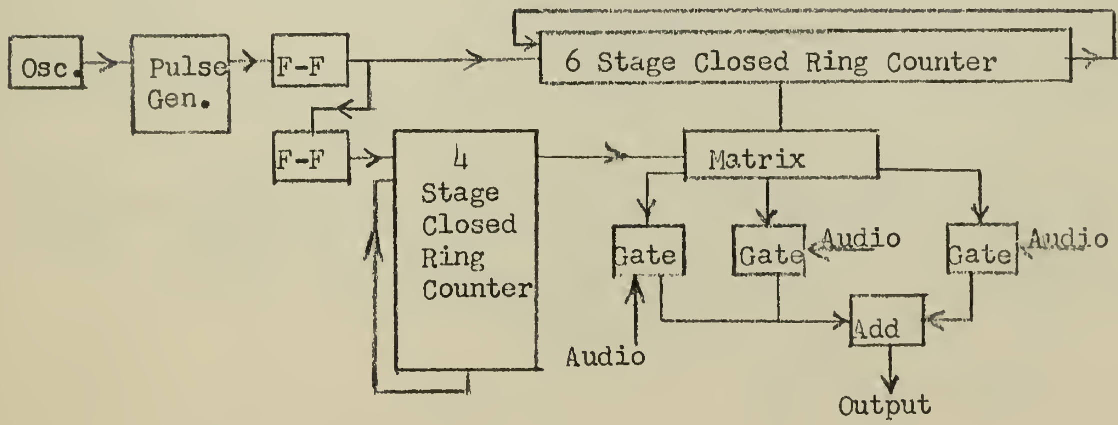


Figure 6a

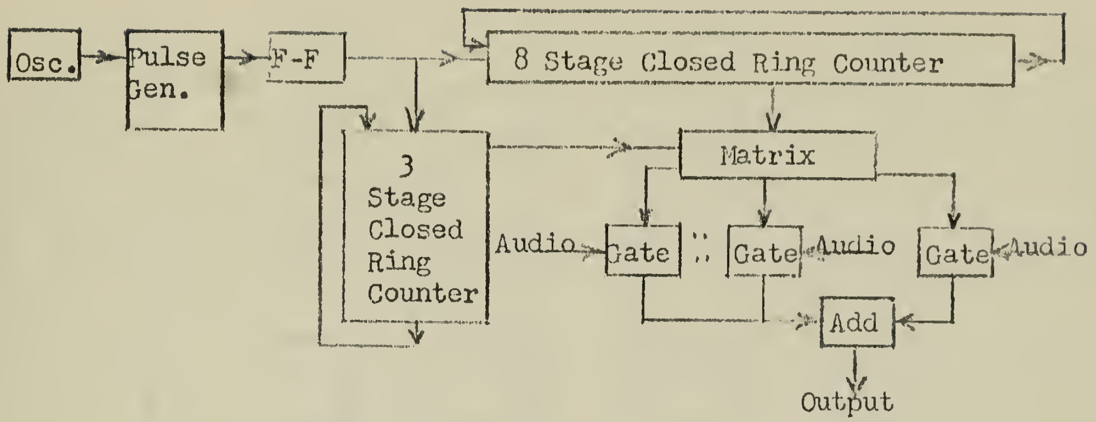


Figure 6b

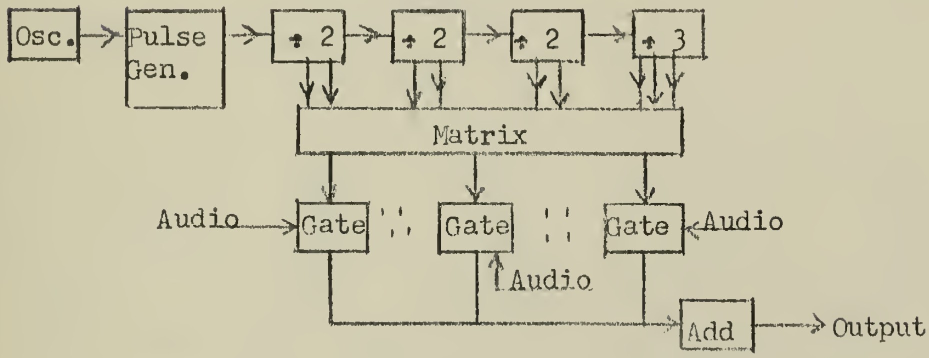


Figure 7a

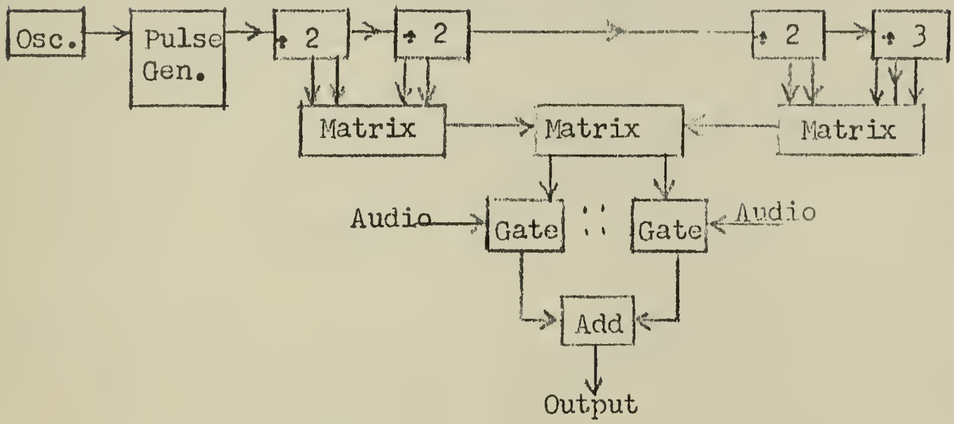


Figure 7b

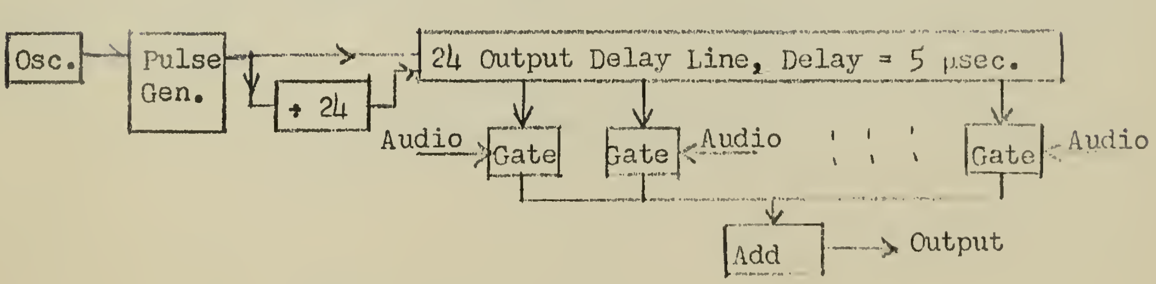
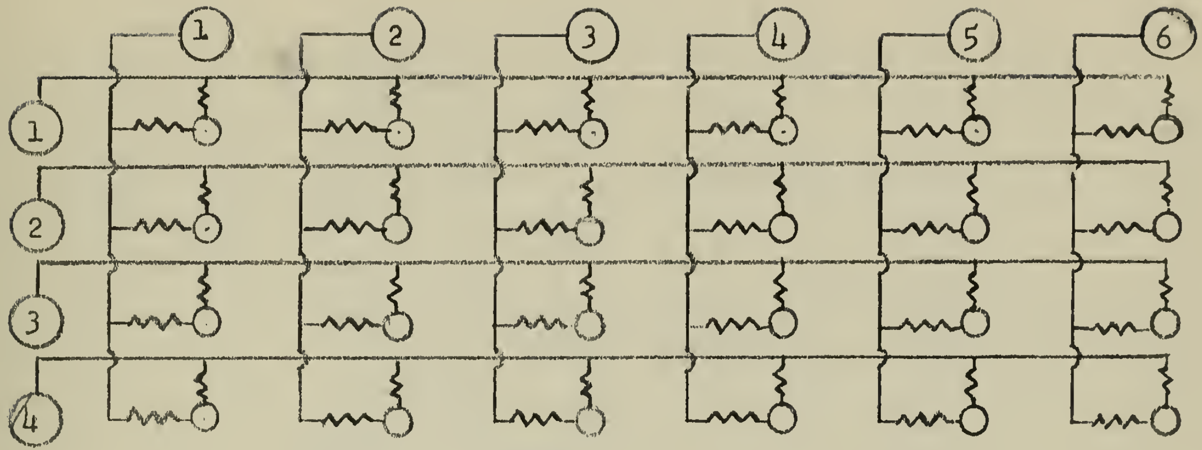


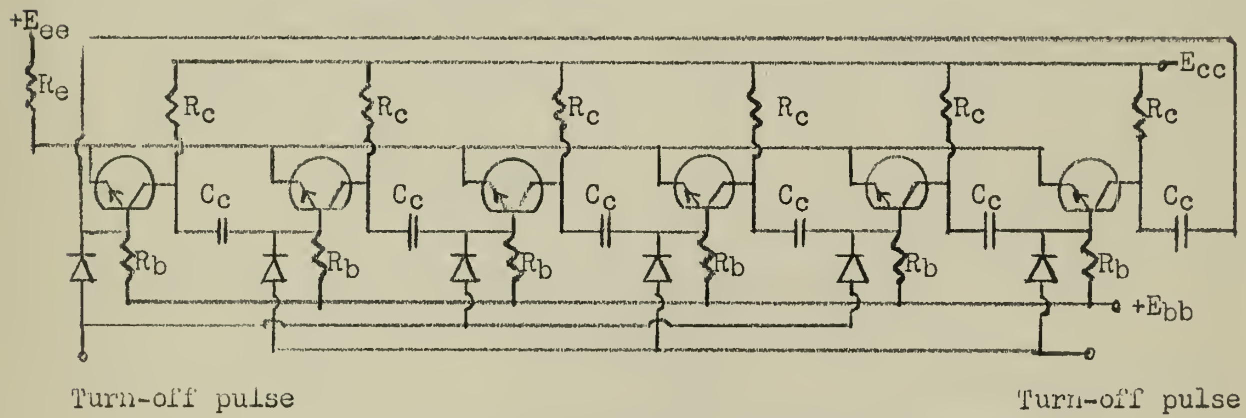
Figure 8



Matrix Configuration

Figure 9

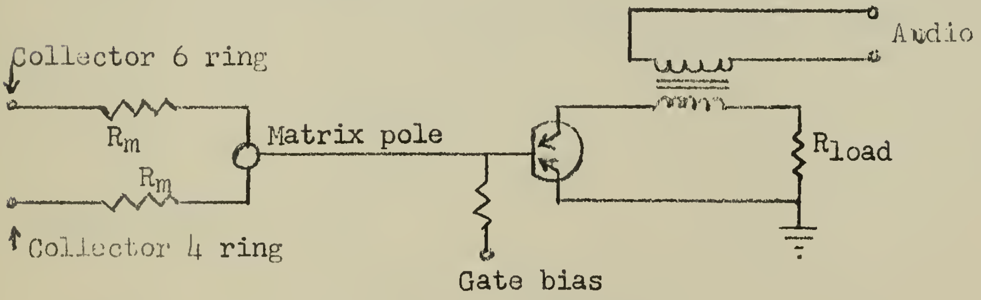
(all resistors = R_m)



(for four ring, delete two stages and close)

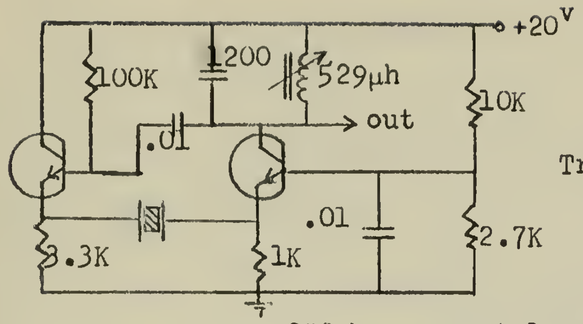
Ring Counter Configuration

Figure 10



Gate Circuit Configuration

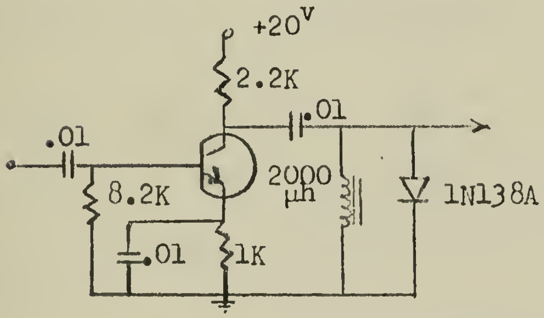
Figure 11



Transistors - T.I.904

200 kcs. Crystal Oscillator

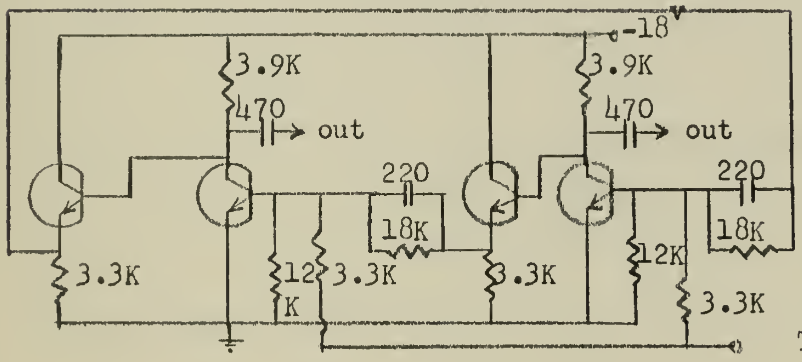
Figure 12



Transistor - T.I. 904

Pulse Generator

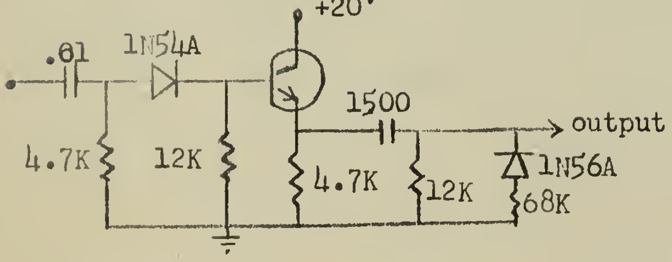
Figure 13



All transistors are
RCA experimental
high frequency
junction units

Flip - flop

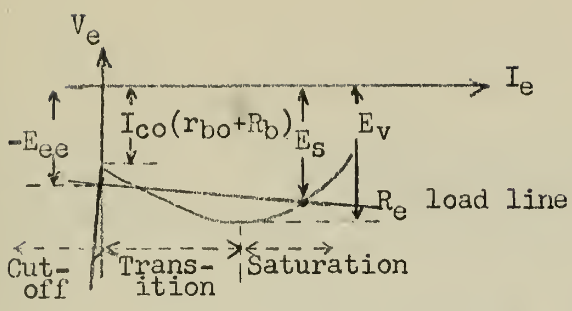
Figure 14



Transistor - T.I. 904

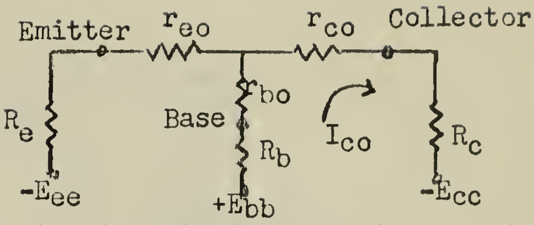
Emitter follower

Figure 15



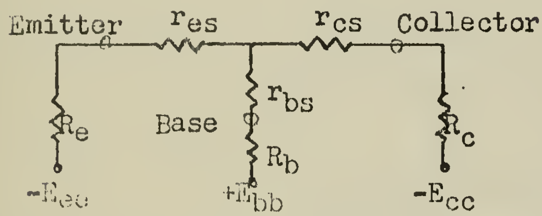
Typical N curve-Pt.contact trans.

Figure 16



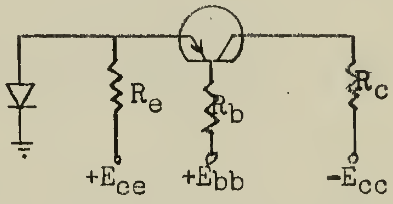
Eq.ckt.-Pt.contact trans. in cut-off

Figure 17



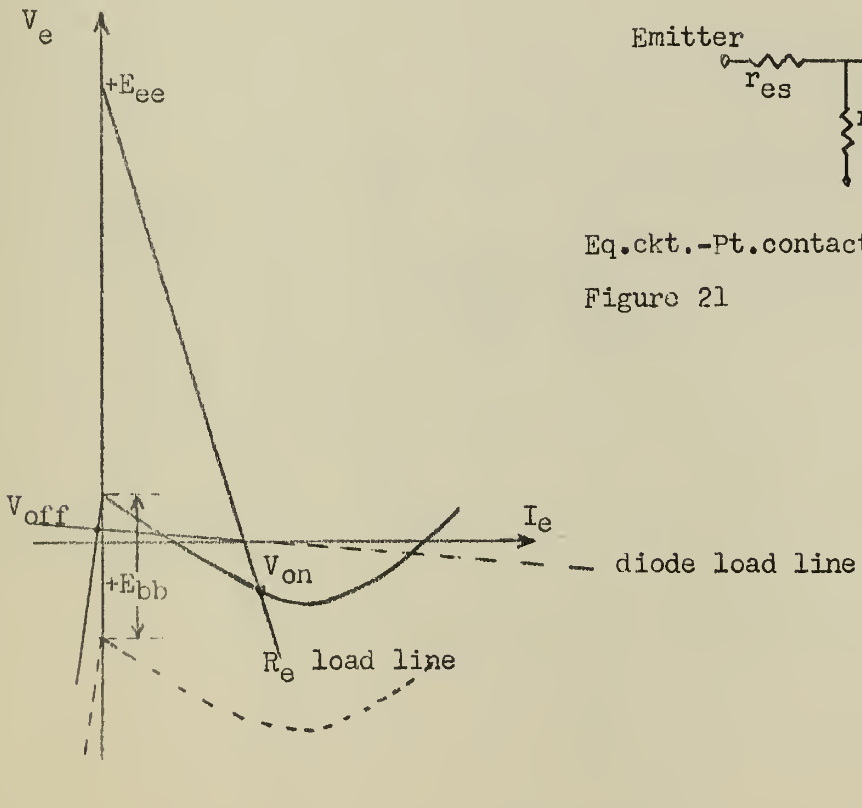
Eq.ckt.-Pt.contact trans.-saturation

Figure 18



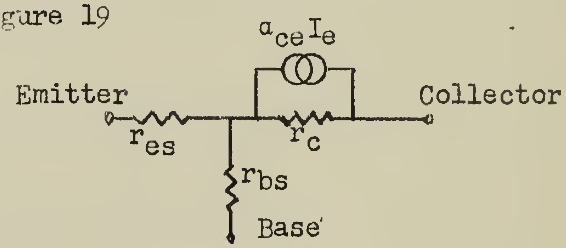
Bistable ckt.using non-linear emitter load

Figure 19



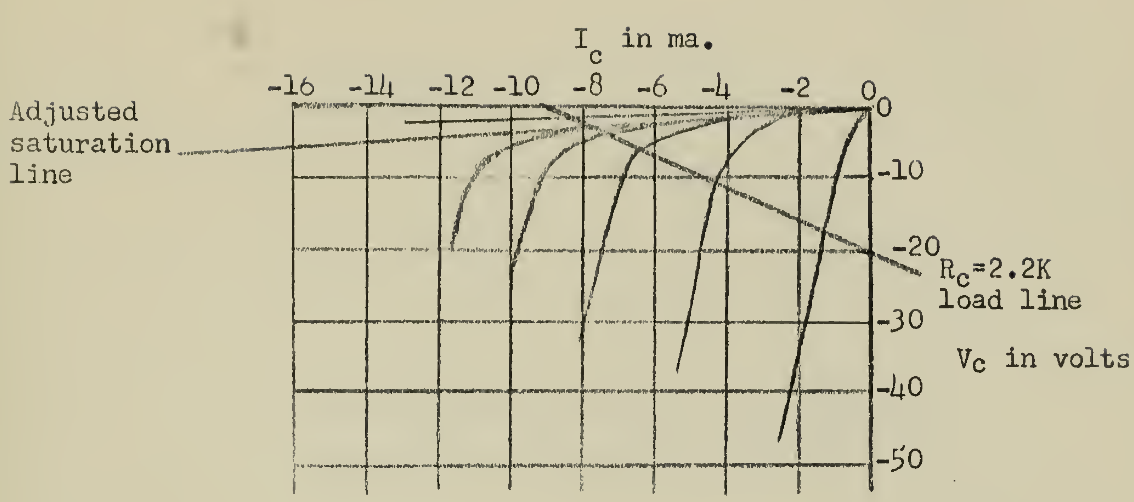
Typical N curve for a non-saturating point contact flip-flop

Figure 20

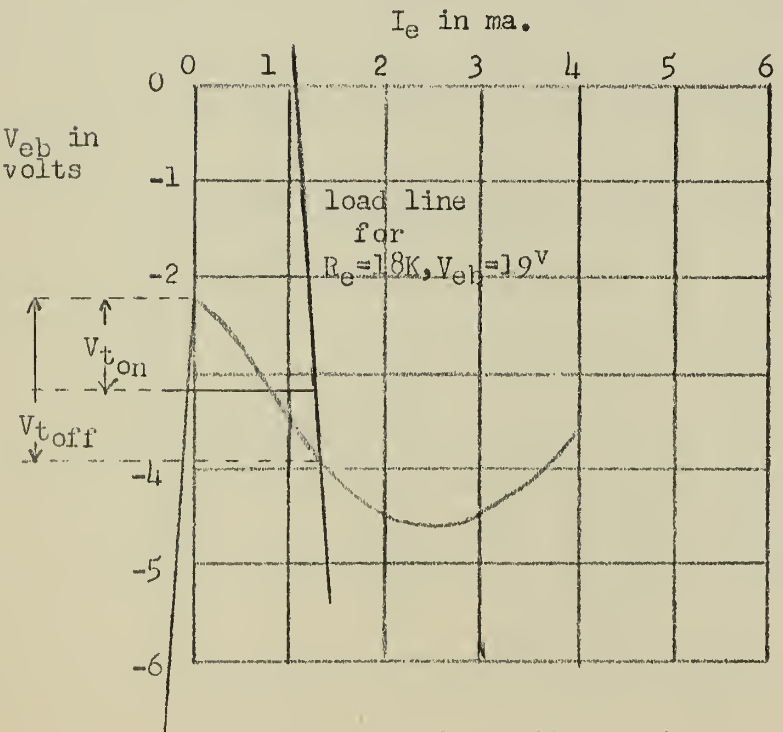


Eq.ckt.-Pt.contact trans.-transition

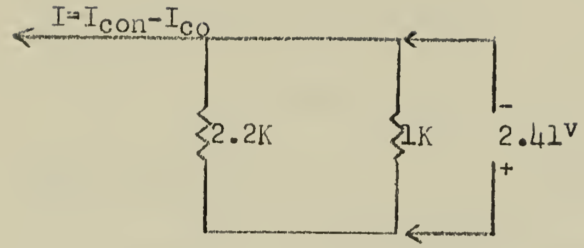
Figure 21



Collector characteristics - 2N22
Figure 22

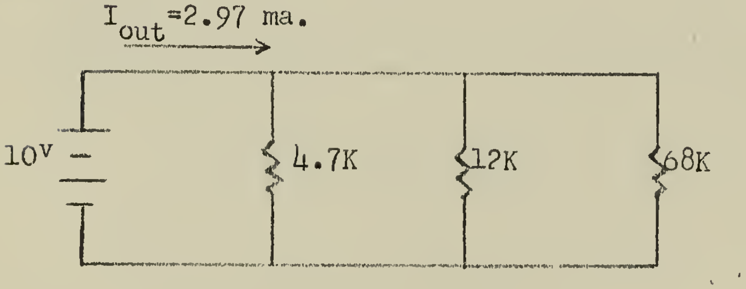


Average N curve for 2N22 transistors with R_b=1K, R_c=2.2K, E_{cc}=-20^V
Figure 23



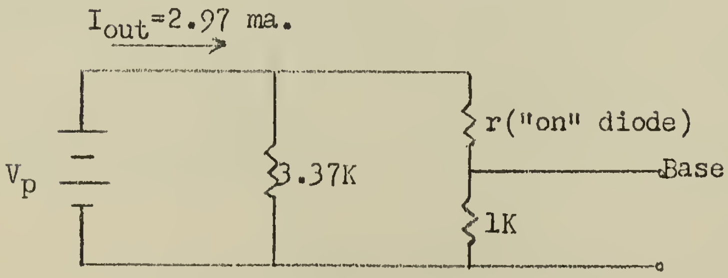
Equivalent output circuit, ring collector

Figure 24



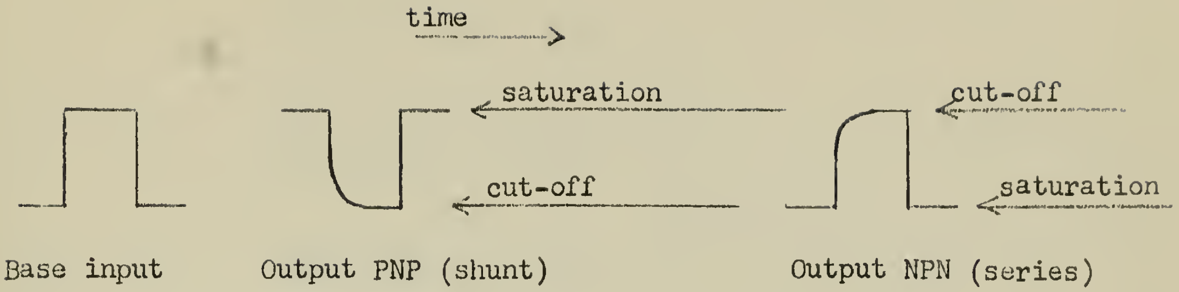
Emitter follower equivalent output circuit-no load

Figure 25



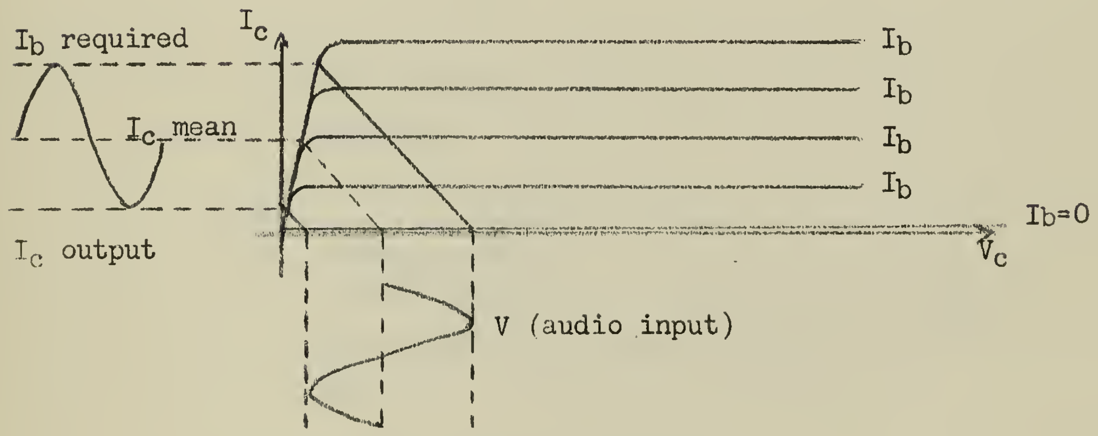
Emitter follower equivalent output circuit-loaded

Figure 26



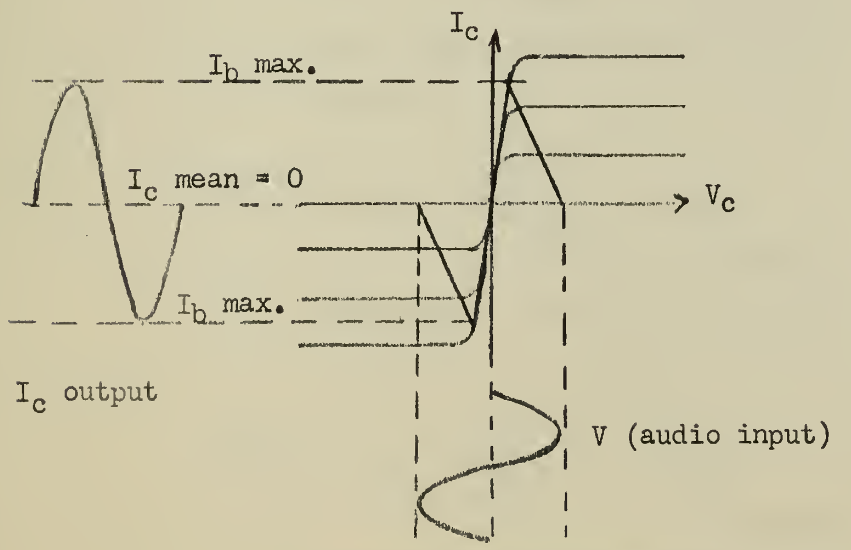
Output waveforms, junction transistors

Figure 27



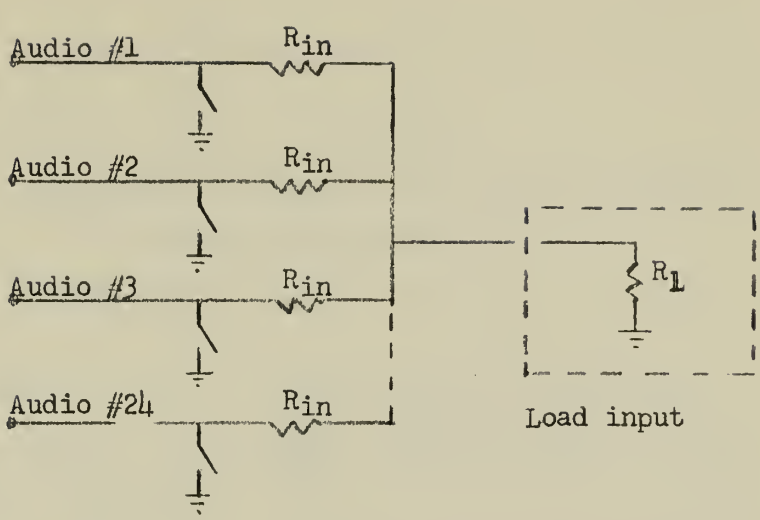
Non-symmetrical gate operation

Figure 28



Symmetrical gate operation

Figure 29

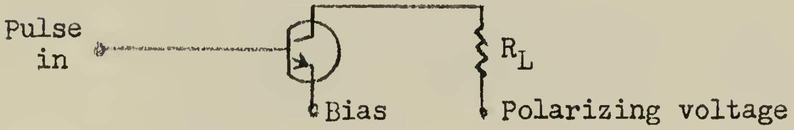


"OR" gate type circuit

Figure 30

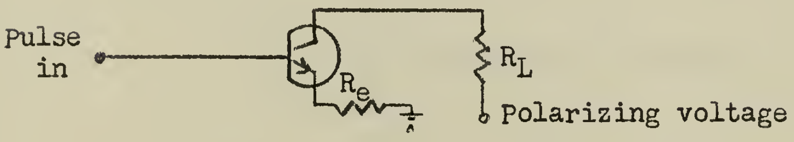
Gate circuit with reverse bias (1)

Figure 31



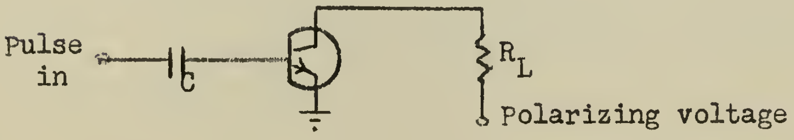
Gate circuit with reverse bias (2)

Figure 32



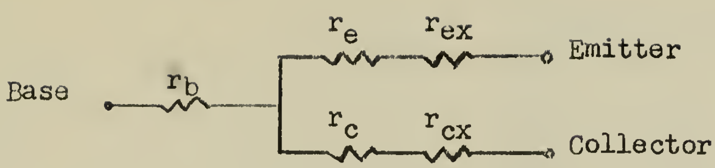
Gate circuit with emitter resistor bias

Figure 33



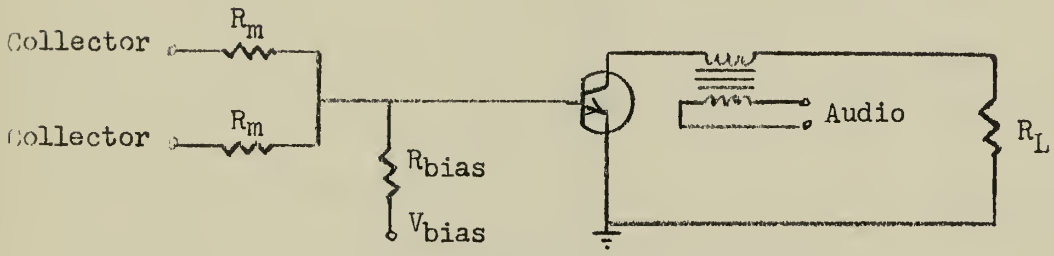
Gate circuit with capacitor input

Figure 34



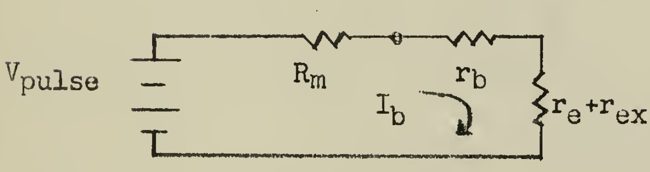
Equivalent circuit of a junction transistor in voltage saturation

Figure 35



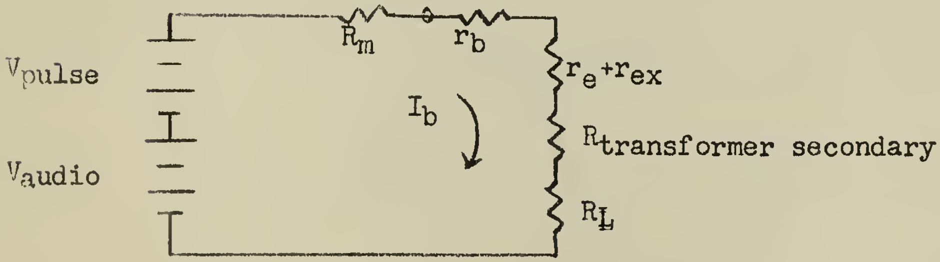
N-P-N symmetrical series gate

Figure 36



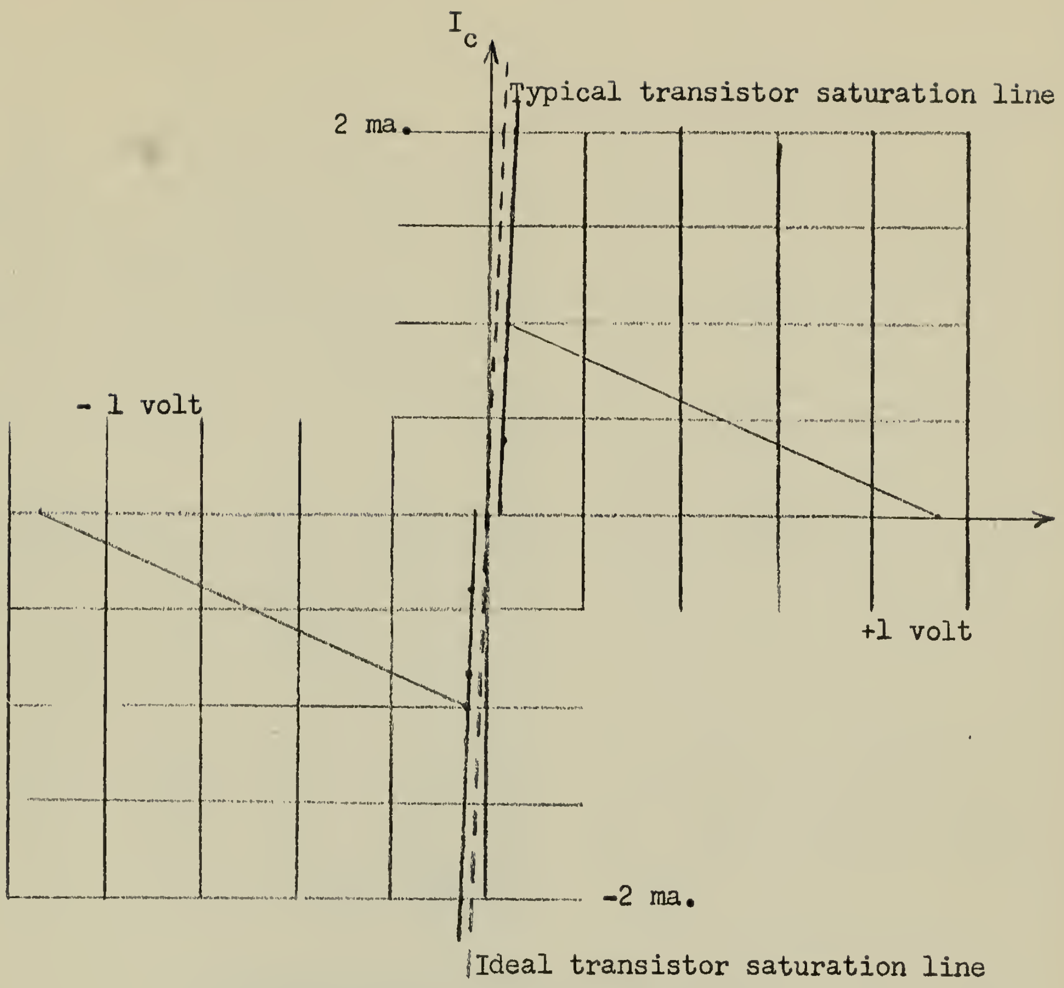
N-P-N symmetrical gate equivalent input circuit for + audio polarity at collector

Figure 37



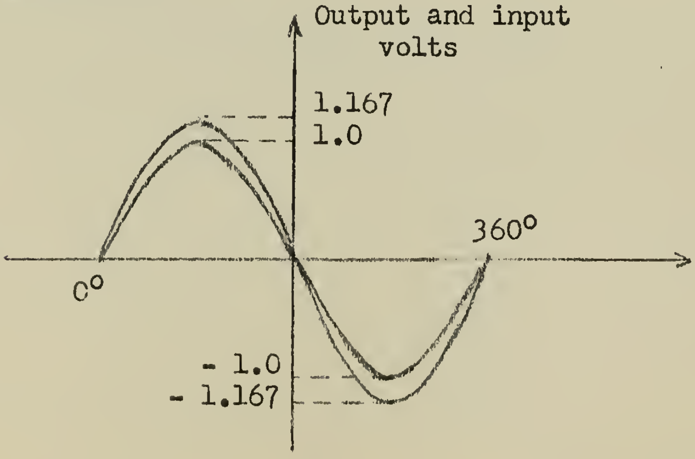
N-P-N symmetrical gate equivalent input circuit for - audio polarity at collector

Figure 38



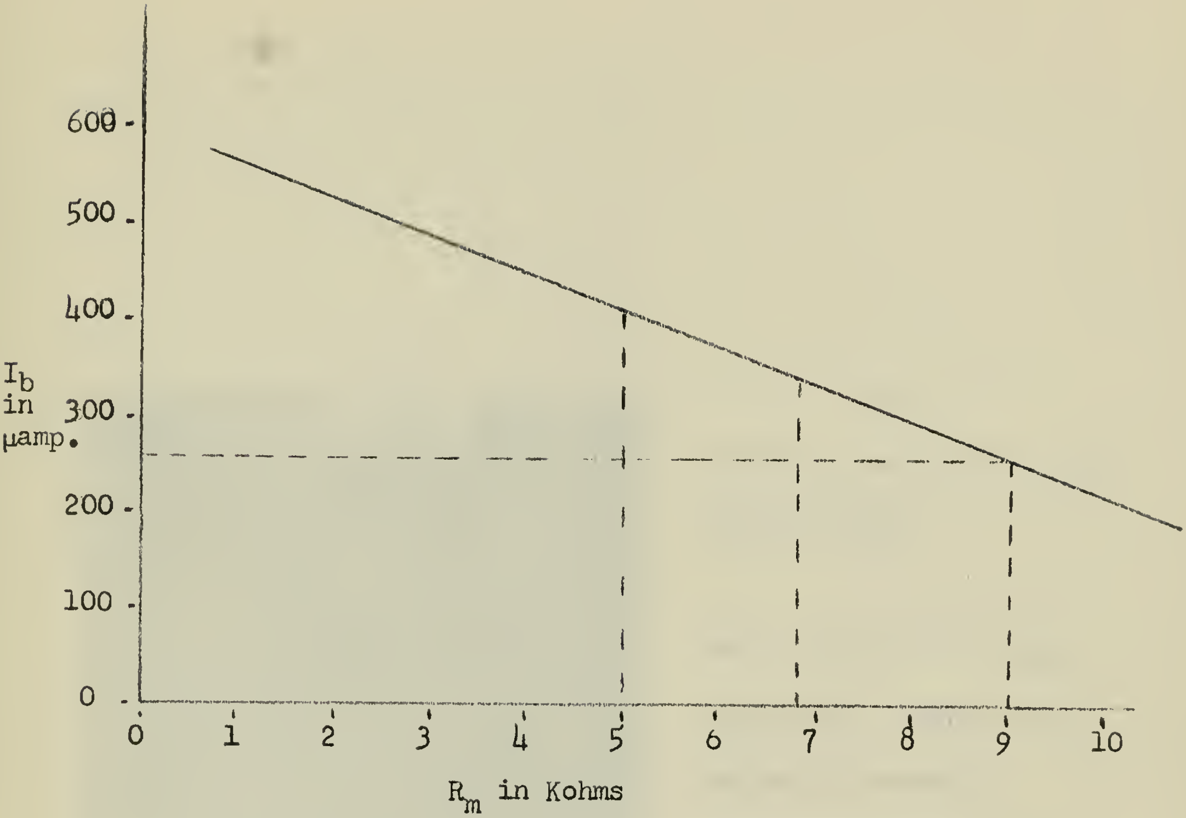
Expanded portion of the foreward and reverse collector characteristics for an average ZJ6 transistor

Figure 39



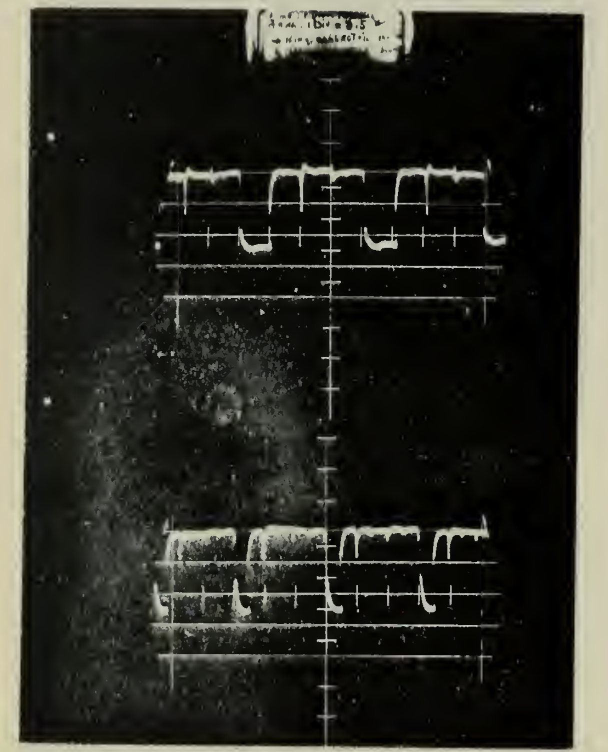
Waveforms from figure 39 used in 5 point analysis

Figure 40



Available gate base current versus matrix resistors

Figure 41



#1

Four Ring Collector - open circuit output

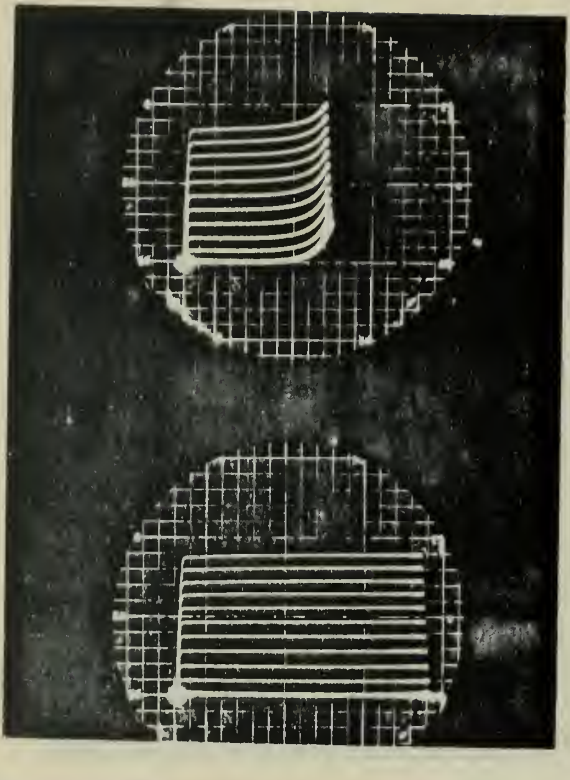
time - 1 div. = 10 μsec.

amplitude - 1 div. = 2.5 V

(polarity inverted)

(time increases to right)

Six Ring Collector - open circuit output



2

Reverse Collector Characteristics

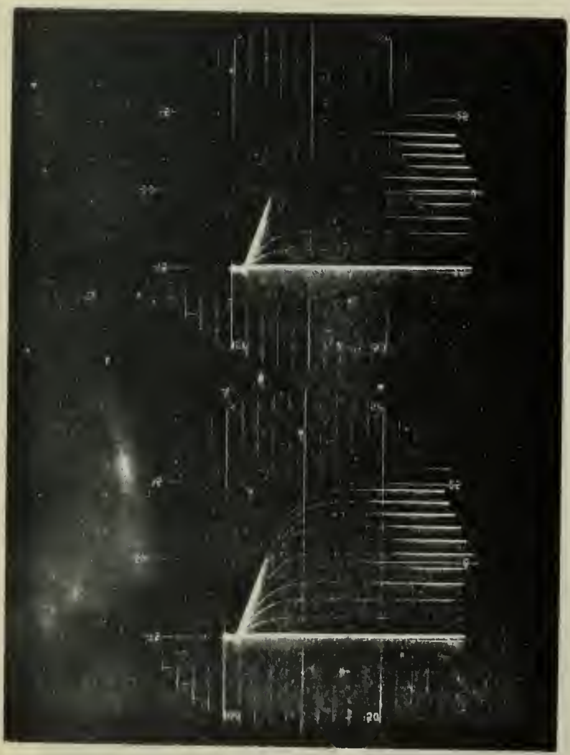
Voltage - 3 div.= 1 volt (horiz)

Current - 3 div. = 1 ma. (vert)

Steps of I_b = 10 μa.

Symmetrical Transistor -
showing Zenner breakdown
of reverse connection

Foreward Collector Characteristics



3

Reverse Collector Characteristics

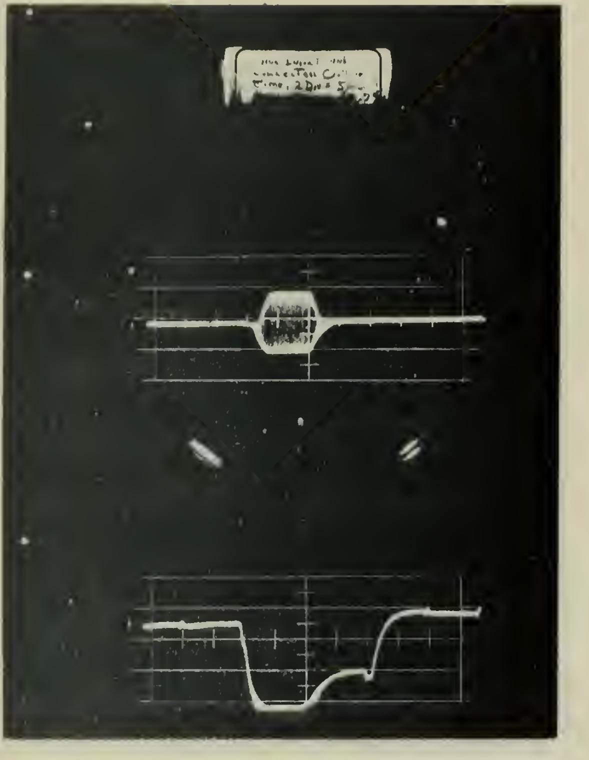
Voltage - 3 div =.1 volt (horiz)

Current - 2.5 div = 1 ma (vert)

Steps of I_b = 25 ma.

Symmetrical Transistor -
(expanded voltage scale)
showing .03 volt jump

Foreward Collector Characteristics



4

Operating Symmetrical

Gate Circuit :

Output Waveform

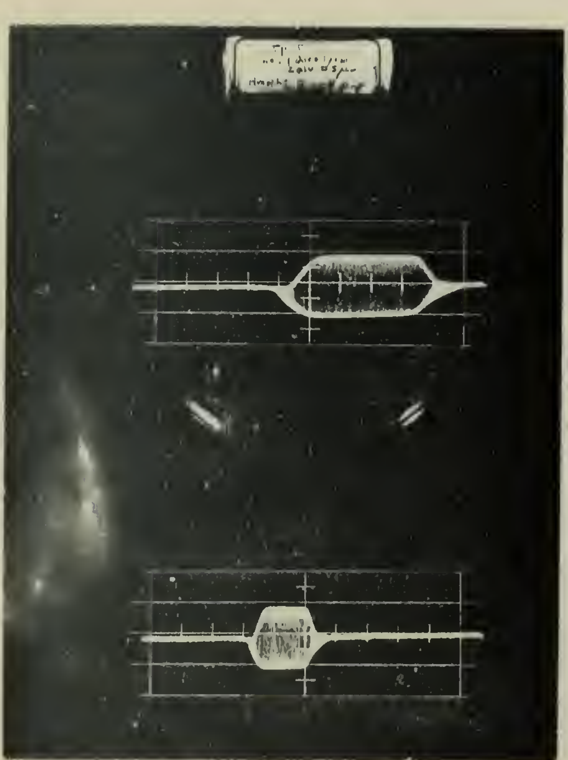
time - 2 div. = 5 μsec.

amplitude - 4 div. = 3.7^{V}

(polarity inverted)

(time increases to right)

Input Waveform



5

Operating Symmetrical

Gate Circuit :

Output Waveform

time - 1 div. = 1 μsec.

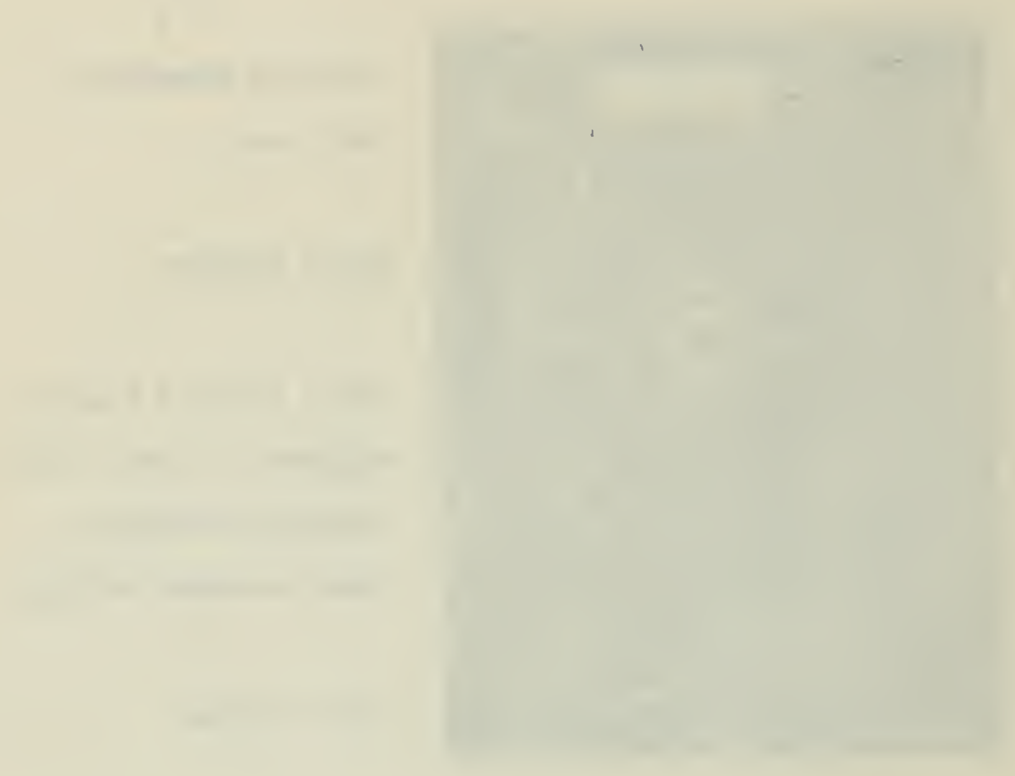
amplitude - 4 div. = 3.7^{V}

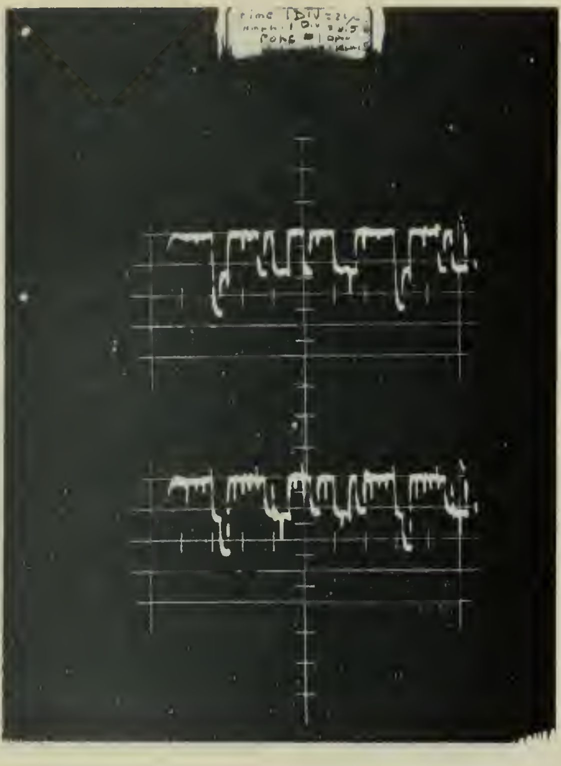
(polarity inverted)

(time increases to right)

Output Waveform

time - 2 div. = 5 μsec.





6

Matrix Outputs -

open circuit

Output - Pole # 1

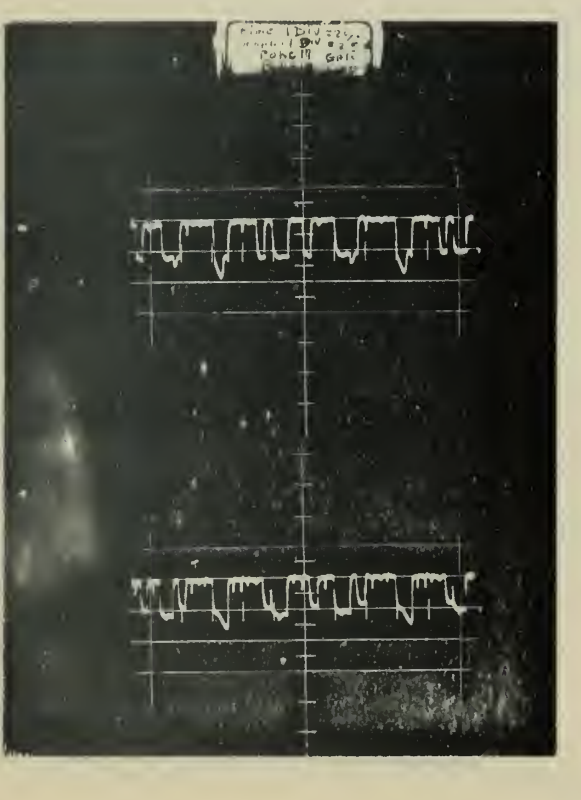
time - 1 div. = 20 μsec.

amplitude - 1 div. = 2.5 V

(polarity inverted)

(time increases to right)

Output - Pole # 2



7

Matrix Outputs -

gate circuit load

Output - Pole # 17

time - 1 div. = 20 μsec.

amplitude - 1 div. = 2.5 V

(polarity inverted)

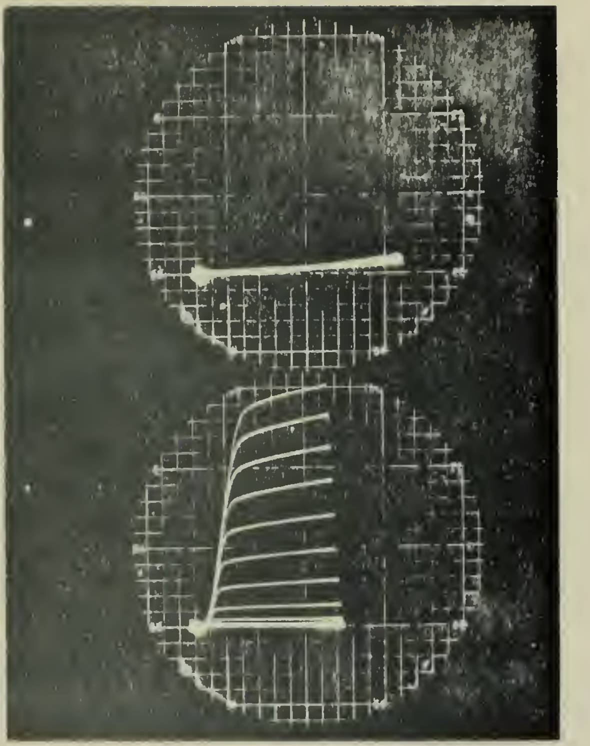
(time increases to right)

Output - Pole # 18

[illegible]

[illegible]

8



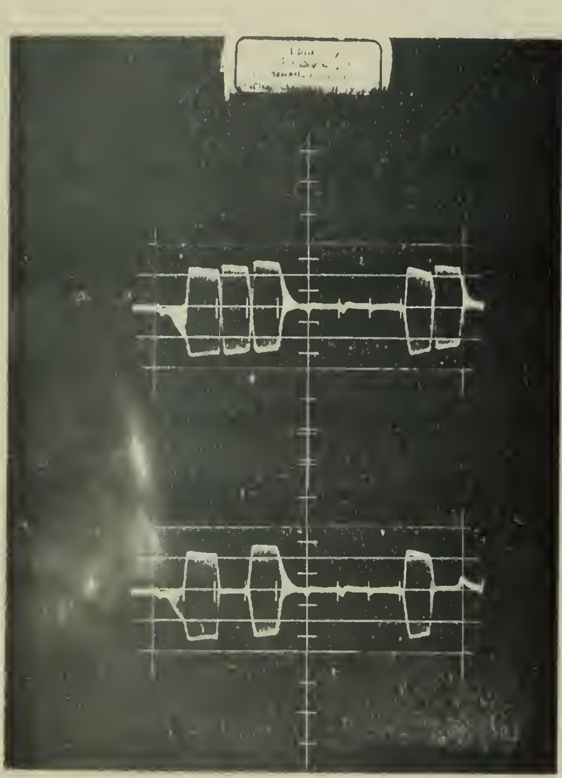
Reverse Collector Characteristics

voltage - 3 div. = 1 volt (horiz)
current - 3 div. = 1 ma. (vert)
steps of I_b = 6 μa.

Silicon Transistor - type 904-A (N-P-N)

Foreward Collector Characteristics

9



Output Waveform for Five Gate Circuits

10, 11, 12, 17, 18 modulating

time - 1 div. = 5 μsec.
amplitude - 1 div. = 2.5 ^{v}
(polarity inverted)
(time increases to right)

10, 12, 17 modulating - No Audio on # 11, 18

BIBLIOGRAPHY

1.	Anderson, A. E.	TRANSISTORS IN SWITCHING CIRCUITS Proc. I.R.E., vol. 40, November 1952
2.	Carlson, A. W.	HIGH SPEED NON-SATURATING FLIP-FLOPS An article in "Symposium on the Application of Transistors to Military Electronic Equipment", MON500-53, September 1953.
3.	Coblenz, A. and Owens, H. L.	VARIATION OF TRANSISTOR PARAMETERS WITH TEMPERATURE Proc. I.R.E., vol. 40, November 1952
4.	Deuitch, D. E.	JUNCTION TRANSISTOR SWITCHING CHARACTERISTICS. Presented at A.I.E.E.-I.R.E. Conference on Transistor Circuits, Philadelphia, February 1954. Soon to be published in Proc. I.R.E.
5.	Giacoletto, J. L.	STUDY OF P-N-P ALLOY JUNCTION TRANSISTORS FROM D-C THROUGH MEDIUM FREQUENCIES RCA Review, Vol. IV, No. 4, December 1954
6.	Lo, A. W.	TRANSISTOR TRIGGER CIRCUITS Proc. I.R.E., vol. 40, November 1952
7.	Moore, A. R. and Pankove, J. I.	THE EFFECT OF JUNCTION SHAPE AND SURFACE RECOMBINATION ON TRANSISTOR CURRENT GAIN Proc. I.R.E., vol. 42, June 1954
8.	Raytheon	FIRST QUARTERLY REPORT ON THE DEVELOPMENT, DESIGN AND CONSTRUCTION OF PPM-AM MULTIPLEX TERMINALS USING TRANSISTORS Period 1 July 1953 to 30 September 1953
9.	Radio Corporation of America	SEMI-ANNUAL REPORT ON TIME DIVISION MULTIPLEX SYSTEMS For period 1 July 1954 to 31 January 1955
10.	Shea, R. F.	TRANSISTOR CIRCUITS, 3rd Printing Wiley, May 1954

11. Sziklai, G. C.   SYMMETRICAL PROPERTIES OF TRANSISTORS
AND THEIR APPLICATIONS
Proc. I.R.E., vol. 41, June 1953

Clarke 29082

A system for producing a pulse amplitude modulated, time division multiplex signal.

29082

Clarke

A system for producing a pulse amplitude modulated, time division multiplex signal.